# Integrating Renewable Energy Sources Using Interleaved Boost Converter For Charging Batteries

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***Abstract*— Solar and wind setups put out variable, low-voltage DC power that needs a solid step-up stage before it can feed into a grid or charge a battery. Standard single-phase boost converters tend to produce a heavy input current ripple, which wears down the source prematurely. Two-phase interleaved boost converters (IBCs) solve this by using phase-shifted switching to cancel out that ripple. But most current IBC control setups focus only on maximum power point tracking (MPPT) for the source, completely ignoring power losses inside the converter itself. To fix this, we propose a time-domain decoupled dual-loop control method for a two-phase IBC built for a 24V to 48V, 100–200W system. Running on an STM32 ARM Cortex-M chip, the control firmware splits into two separate loops: a P&O MPPT routine that runs every 100 ms to handle source optimization, and an efficiency optimizer running every 500 ms that tweaks the steady-state duty cycle by $\pm 0.2\%$ to cut down on conduction and switching losses. We tested the dynamic stability and ripple reduction using MATLAB/Simulink SimPowerSystems. The simulations show stable 48V output regulation and clean ripple cancellation with zero loop interference. We also outline a full hardware layout using custom magnetics and high-speed gate drivers for future physical testing.**

**Keywords-** *Interleaved Boost Converter, Maximum Power Point Tracking, Dual-Loop Control, Renewable Energy, STM32, Efficiency Optimization, Phase-Shifted PWM, Time Domain Decoupling, Energy Conversion Efficiency.*

## I. INTRODUCTION

The shift toward decentralized renewable energy generation is pushing the rapid adoption of solar photovoltaic (PV) systems, micro-wind turbines, and fuel cells. These setups typically generate variable, low-voltage DC power (roughly 12V to 24V) that has to be stepped up and conditioned to a clean 48V for battery storage and DC microgrids.

Single-phase DC-DC boost converters are commonly used because they are straightforward to build. However, they suffer from a major operational flaw: high-frequency input current ripple. When this raw ripple feeds straight into solar cells or fuel cell membranes, it causes localized heating and shortens their lifespan. It also knocks the source off its Maximum Power Point (MPP) on the I-V curve, which drops overall energy extraction efficiency. To filter out these stresses, single-phase designs require massive, expensive input capacitors that destroy the converter's power density.

Interleaved Boost Converters (IBCs) offer a solid structural fix. By putting two or more boost stages in parallel and driving the switches with a precise phase shift (180° for a two-phase setup), the high-frequency inductor ripples cancel each other out right at the common input node. This multiphase approach drastically drops the net input ripple, eases current stress on the MOSFETs, and shrinks the needed filter sizes.

Despite these structural benefits, current control methods have a blind spot. Most embedded systems focus entirely on source-side dynamics, running standard Maximum Power Point Tracking (MPPT) like Perturb and Observe. They completely ignore internal power losses inside the converter itself—such as switching losses, diode reverse-recovery, and inductor conduction losses—which shift constantly with the duty cycle and load profile. Ignoring internal losses means leaving real efficiency gains unrealized.

To bridge this gap, this paper introduces a time-domain decoupled dual-loop control architecture for a two-phase IBC. Our goal is to optimize both source-side power extraction and internal converter efficiency without causing control loop instability.

The key contributions of this work include:

- A dual-loop control strategy that physically separates MPPT tracking and efficiency optimization in the time domain to stop them from interfering with each other.
- An active Efficiency Optimizer loop that calculates real-time power conversion ratios ($P_{out}/P_{in}$) to dynamically fine-tune the steady-state duty cycle.
- A firmware build deployed on an STM32 ARM Cortex-M microcontroller, using advanced hardware timers to keep 180° phase-shifted PWM generation locked in.

- Full theoretical and dynamic validation using MATLAB/Simulink SimPowerSystems, demonstrating stable 48V output regulation and active input ripple cancellation under variable load conditions.

## II. LITERATURE SURVEY

To see where our dual-loop design fits in, we need to look at how others have tackled power optimization and control for Interleaved Boost Converters (IBCs). Past research generally splits into three main areas:

### *A. Source-Side Optimization and MPPT Constraints*

Most research on IBCs tied to renewables focuses strictly on pulling maximum power from the source. Sheik et al. demonstrated how a basic Perturb and Observe (P&O) algorithm works inside an IBC to boost solar PV extraction. Even so, their setup only chased raw input power, completely skipping internal switching and conduction losses that shift with the duty cycle. Similarly, Kumar implemented a variable-step P&O method to cut down input ripple during tracking. While that improved stability, the system had zero real-time efficiency tracking. Pushing the hardware further, Subramanian et al. used a 32-bit ARM Cortex-M processor for fast MPPT execution, but the firmware was locked entirely onto source-side tracking, leaving internal thermal losses unmonitored.

### *B. Topological Performance and Output Regulation*

Beyond tracking algorithms, a lot of work looks at output regulation and system stability. Muthuramalingam et al. used a classical double-feedback setup targeting output voltage and current to keep the DC bus steady. Sahu and Dash and Ahmed broke down the differences between single-phase and interleaved converters, proving that interleaving cuts down high-frequency input ripple and electromagnetic interference (EMI). Even so, these systems used static control logic for conversion and lacked an adaptive software routine to suppress thermal losses when loads shifted.

### *C. Efficiency Tracking and Control Instability*

Recent studies have tried tackling internal converter efficiency, but with clear limits. Zhang et al. shifted switching frequencies dynamically using look-up tables to lower losses at light loads. Relying on a static math model fails when components degrade over time, and changing the frequency on the fly ruins the 180° phase-shift sync needed for clean interleaving. On the other hand, Choudhury et al. used precision shunts to measure input-output efficiency directly in real-time. While accurate, that setup was built for non-interleaved converters and ignored multiphase ripple dynamics. Furthermore, as Santos et al. pointed out regarding P&O limit cycle oscillations, running multiple optimization routines at once without clear time-domain separation usually triggers severe system oscillations and instability.

### *D. Research Gap Synthesis*

A critical review of the literature reveals a distinct operational gap. Existing control strategies either exclusively optimize source-side extraction (MPPT) or attempt static, offline efficiency improvements. No current methodology successfully integrates an active, real-time efficiency optimization loop with a fast-acting MPPT algorithm in a multiphase topology without causing control loop interference. This establishes the direct necessity for a time-domain decoupled control architecture, enabling simultaneous optimization of both the renewable source and the internal conversion stage.

## III. WORKING PRINCIPLE OF IBC

The fundamental operational theory of the Interleaved Boost Converter (IBC) is derived from the conventional step-up boost topology. While a standard boost converter utilizes a single magnetic storage element, the IBC architecture distributes the power conversion process across two parallel branches. This parallel configuration significantly reduces the physical sizing requirements of the individual inductors, splits the thermal stress, and attenuates the net input current ripple.

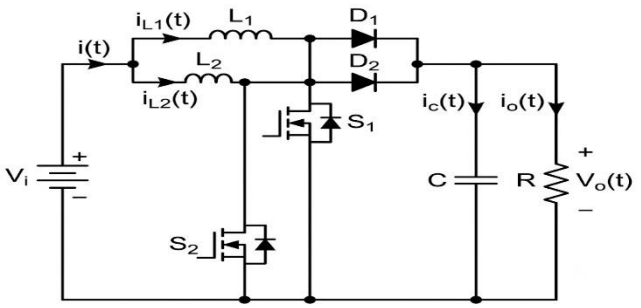


**Fig.1**. Circuit diagram of IBC

The proposed system operates in Continuous Conduction Mode (CCM) with a fixed 180° phase shift ($\varphi = 180°$) applied between the switching signals of the active switches, $S_1$ and $S_2$. To analyze the system dynamically, the operational cycle is divided into distinct switching states.

### *A. Mode 1 Analysis ($S_1$ is ON, $S_2$ is OFF)*

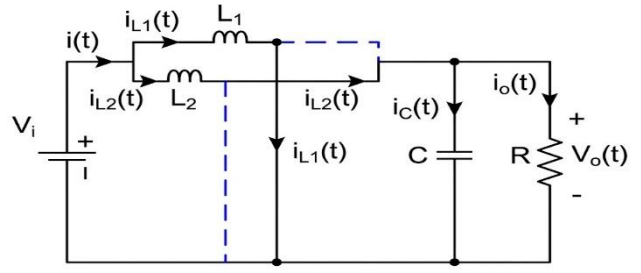


**Fig. 2(a).** Equivalent circuit during Mode 1

In this state, switch $S_1$ is closed, allowing inductor $L_1$ to charge directly from the input DC source ($V_{in}$). Simultaneously, switch $S_2$ is open, forcing inductor $L_2$ to discharge its stored energy through its forward-biased diode into the output capacitor ($C$) and the load ($R$). Applying Kirchhoff's Voltage Law (KVL) to the inductor loops and Kirchhoff's Current Law (KCL) at the output node, the continuous-time dynamic equations are defined as:

$$v_{L1}(t) = V_{in} \tag{1}$$

$$v_{L2}(t) = V_{in} - v_{out}(t) \tag{2}$$

$$i_{in}(t) = i_{L1}(t) + i_{L2}(t) \tag{3}$$

$$i_c(t) = i_{L2}(t) - \frac{v_{out}(t)}{R} \quad (4)$$

*B. Mode 2 Analysis ($S_1$ is OFF, $S_2$ is ON)*

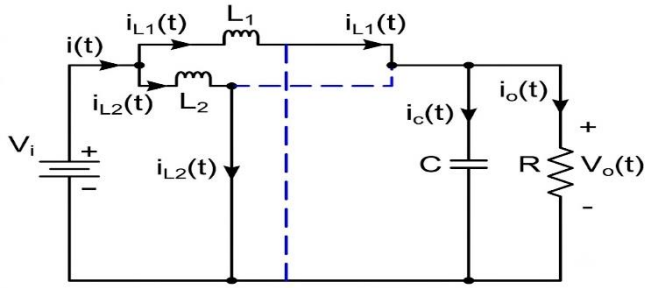


**Fig. 2(b).** Equivalent circuit during Mode 2

In the subsequent state, the switching roles reverse due to the 180° phase shift. Inductor $L_1$ now discharges its energy into the load, while inductor $L_2$ charges directly from the input source. The governing state-space equations become:

$$v_{L1}(t) = V_{in} - v_{out}(t) \quad (5)$$

$$v_{L2}(t) = V_{in} \quad (6)$$

$$i_{in}(t) = i_{L1}(t) + i_{L2}(t) \quad (7)$$

$$i_c(t) = i_{L1}(t) - \frac{v_{out}(t)}{R} \quad (8)$$

*C. Volt-Second Balance and Voltage Gain*

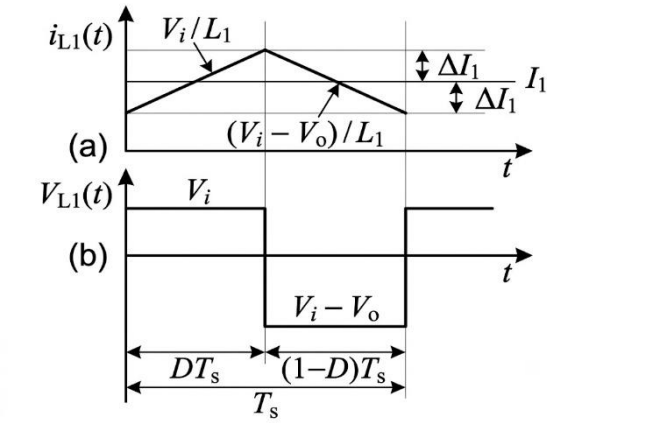


**Fig. 3.** Theoretical waveform showing inductor voltage and current ripple

To determine the ideal steady-state DC transfer function, the small-ripple approximation is applied. This assumes the output voltage ripple is negligible compared to its DC component ($V_{out}$). Therefore, the discrete voltage states across inductor $L_1$ during the ON and OFF periods simplify to:

$$V_{L1_ON} = V_{in} \quad (9)$$

$$V_{L1_OFF} = V_{in} - V_{out} \quad (10)$$

According to the principle of inductor volt-second balance, the integral of the inductor voltage over one complete steady-state switching period ($T_s$) must equal zero:

$$\int_0^{T_s} v_{L1}(t)dt = 0 \quad (11)$$

Splitting the integral into the switch ON-time (0 to $DT_s$) and OFF-time ($DT_s$ to $T_s$):

$$\int_0^{DT_s} V_{L1_ON}\, dt + \int_{DT_s}^{T_s} V_{L1_OFF}\, dt = 0 \quad (12)$$

Evaluating the integrals yields:

$$V_{in}(DT_s) + (V_{in} - V_{out})(T_s - DT_s) = 0 \quad (13)$$

Factoring out $T_s$ from the equation:

$$\frac{1}{T_s}[V_{in}DT_s + (V_{in} - V_{out})(1 - D)T_s] = 0 \quad (14)$$

Dividing through by $T_s$:

$$V_{in}D + (V_{in} - V_{out})(1 - D) = 0 \quad (15)$$

Expanding the terms algebraically:

$$V_{in}D + V_{in} - V_{in}D - V_{out}(1 - D) = 0 \quad (16)$$

Cancelling the $V_{in}D$ terms:

$$V_{in} = V_{out}(1 - D) \quad (17)$$

Solving for the output voltage yields the ideal steady-state voltage gain of the converter:

$$V_{out} = \frac{V_{in}}{1-D} \quad (18)$$

*D. Component Sizing*

The design of the passive components is critical to maintaining CCM operation. The voltage across an inductor is defined fundamentally as:

$$v_L = L\frac{di_L}{dt} \quad (19)$$

Applying this to the switch ON-time, where the current rises by $\Delta I_{L1}$ over duration $DT_s$:

$$V_{in} = L_1\frac{\Delta I_{L1}}{DT_s} \quad (20)$$

Rearranging to solve for the peak-to-peak inductor current ripple, where switching frequency $f_s = 1/T_s$:

$$\Delta I_{L1} = \frac{V_{in}DT_s}{L_1} = \frac{V_{in}D}{f_s L_1} \quad (21)$$

Similarly, the output filtering capacitance ($C$) required to limit the steady-state output voltage ripple ($\Delta V_{out}$) is determined by analyzing the charge ($\Delta Q$) depleted by the load during the switch ON-time:

$$C = \frac{V_{out}D}{Rf_s\Delta V_{out}} \quad (22)$$

## IV. PROPOSED RENEWABLE ENERGY INTEGRATION AND CONTROL ARCHITECTURE

Integrating a non-linear renewable energy source, such as a Photovoltaic (PV) array, with an Interleaved Boost Converter requires a sophisticated control mechanism. Because PV arrays exhibit variable Power-Voltage (P-V) characteristics dependent on fluctuating environmental conditions (irradiance and temperature), the converter must continuously adjust its input impedance to track the Maximum Power Point (MPP).

To achieve optimal source extraction while maintaining internal converter stability, this paper proposes a time-domain decoupled dual-loop control strategy executed via an STM32 microcontroller. By isolating the maximum power extraction algorithms from the high-frequency phase-current regulation, this architecture effectively mitigates limit-cycle oscillations commonly observed in conventional single-loop topologies. Consequently, the controlled energy transfer not only maximizes the utilization of the solar array but also yields a highly regulated, low-ripple DC output, making the proposed system specifically well-suited for reliable battery charging applications and continuous energy storage.

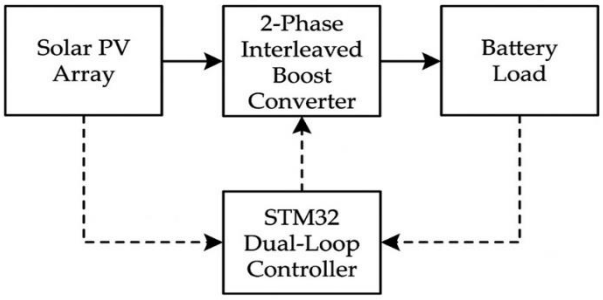


**Fig. 4.** Proposed system block diagram integrating the PV array, IBC, and STM32 control loops

### *A. The Necessity of Time-Domain Decoupling*

Traditional MPPT implementations often suffer from control loop interference when applied to multiphase converters. If the algorithm attempting to maximize source power runs concurrently at the same execution speed as the algorithm managing the internal phase currents, the system experiences severe limit-cycle oscillations. To resolve this, the proposed architecture separates the control objectives in the time domain, assigning distinct execution frequencies to the outer and inner control loops.

### *B. Outer Loop: MPPT (Slow Execution Dynamics)*

The outer control loop is strictly dedicated to source-side optimization. A standard MPPT algorithm (such as Perturb and Observe) continuously samples the PV array voltage ($V_{pv}$) and current ($I_{pv}$) to calculate instantaneous power. Because environmental changes (cloud cover, temperature shifts) occur relatively slowly, this outer loop is designed to execute at a low frequency (e.g., 10 Hz to 50 Hz). This deliberate delay ensures the MPPT algorithm only reacts to genuine environmental shifts rather than transient switching noise, establishing the baseline reference duty cycle ($D_{ref}$) for maximum power extraction.

### *C. Inner Loop: Phase Balancing (Fast Execution Dynamics)*

Conversely, the inner control loop governs the high-frequency dynamics of the IBC. Its primary objective is to maintain identical current sharing between inductor $L_1$ and $L_2$ and to enforce the precise 180° phase shift. Because internal component variations and switching transients occur instantaneously, this loop executes at the switching frequency of the converter (e.g., 20 kHz to 100 kHz). By operating magnitudes faster than the outer MPPT loop, the inner loop dynamically fine-tunes the duty cycles ($D_1$ and $D_2$) around the baseline $D_{ref}$ without interfering with the solar tracking algorithm.

### *D. Proposed Firmware Implementation via STM32*

The hardware realization of this decoupled architecture is proposed using an STM32 32-bit microcontroller. The STM32 architecture is specifically selected for its Advanced Control Timers and high-speed Analog-to-Digital Converters (ADCs). The firmware utilizes the Nested Vectored Interrupt Controller (NVIC) to enforce the time-domain decoupling. The fast inner loop is triggered via high-priority hardware timer interrupts, ensuring real-time phase balancing, while the slower MPPT loop operates as a low-priority background task. This proposed architecture guarantees that the mathematical extraction of maximum renewable power never compromises the electrical stability of the two-phase interleaved hardware.

## V. DUAL LOOP CONTROL STRATEGY

The theoretical execution of the time-domain decoupled control architecture relies on the precise management of microcontroller peripherals. The STM32 dynamically allocates processing bandwidth between the slow-moving Maximum Power Point Tracking (MPPT) constraints and the fast-moving phase current regulation, preventing algorithmic interference.

### *A. Interrupt Priority Logic*

The proposed firmware architecture utilizes the Nested Vectored Interrupt Controller (NVIC) intrinsic to the ARM Cortex core of the STM32. To enforce the decoupling strategy, strict preemption priorities must be assigned. The inner current-balancing loop is triggered by a high-priority hardware timer interrupt, executing exactly at the fundamental switching frequency of the converter ($f_{sw}$). Conversely, the outer MPPT loop operates as a low-priority periodic background task. If an MPPT calculation is actively processing when a timer interrupt triggers, the NVIC immediately suspends the MPPT task, seamlessly services the phase-current balancing routine to update the PWM channels, and subsequently resumes the MPPT calculation. This preemptive logic ensures

that critical high-frequency switching events are never delayed by complex mathematical operations.

### *B. Shared Duty Cycle Register*

Data transfer between the asynchronous control loops is handled via a shared volatile memory register containing the reference duty cycle ($D_{ref}$). The slow outer MPPT algorithm acts as the system master, continuously calculating the optimal voltage operating point based on solar irradiance and updating the $D_{ref}$ variable. The fast inner loop acts as the slave, pulling the most recent value of $D_{ref}$ during every switching cycle.

To achieve precise phase balancing, the inner loop senses the instantaneous currents of both inductors ($i_{L1}$ and $i_{L2}$). If an imbalance is detected ($\Delta i = i_{L1} - i_{L2} \neq 0$), a discrete Proportional-Integral (PI) control law generates a localized compensation factor ($\Delta D$). The individual duty cycles for the two converter phases are then dynamically adjusted around the reference baseline:

$$D_1 = D_{ref} - \Delta D \tag{23}$$

$$D_2 = D_{ref} + \Delta D \tag{24}$$

### *C. Time-Domain Decoupling Execution*

By deliberately restricting the update rate of $D_{ref}$ to match slow environmental dynamics (e.g., execution at 10 Hz) while processing the active phase duty cycles ($D_1$ and $D_2$) at the high-speed switching frequency (e.g., 50 kHz), the system achieves true time-domain decoupling. The MPPT algorithm evaluates the entire Interleaved Boost Converter as a single, unified equivalent load, operating entirely oblivious to the high-speed internal current-sharing mechanics occurring between the individual phases.

## VI. PERTURB & OBSERVE (P&O) ALGORITHM MECHANICS

To maximize power extraction from the Solar PV array, a robust tracking mechanism is required to dynamically locate the Maximum Power Point (MPP) on the non-linear Power-Voltage (P-V) curve. The proposed system employs the Perturb and Observe (P&O) algorithm due to its computational efficiency and its seamless integration with the previously defined time-domain decoupling strategy.

### *A. Mathematical Mechanics*

The core principle of the P&O method is to introduce a deliberate, periodic perturbation into the system's operating voltage and observe the resulting change in output power. The discrete-time algorithmic execution begins by sampling the instantaneous voltage, $V(k)$, and current, $I(k)$, from the PV array at the current sampling instant $k$. The instantaneous power is calculated as:

$$P(k) = V(k) \cdot I(k) \tag{25}$$

The controller then calculates the differential changes in power ($\Delta P$) and voltage ($\Delta V$) relative to the previous sampling instant, $k-1$:

$$\Delta P = P(k) - P(k-1) \tag{26}$$

$$\Delta V = V(k) - V(k-1) \tag{27}$$

The fundamental objective of the algorithm is to iteratively drive the system toward the peak of the P-V curve, satisfying the condition where the derivative of power with respect to voltage is zero ($dP/dV = 0$).

### *B. Algorithmic Flowchart Logic*

The decision-making matrix of the P&O algorithm dictates the directional adjustment of the reference variable. Because the input voltage of a Boost Converter is inversely proportional to its duty cycle ($D$), the logic matrix translating the perturbation into the shared reference register ($D_{ref}$) operates as follows:

- Positive Power Gradient **($\Delta P > 0$):** The previous perturbation successfully moved the operating point closer to the MPP. The algorithm maintains the direction of that perturbation.
- If $\Delta V > 0$, the voltage must be increased further. The controller *decreases* the reference duty cycle: $D_{ref}(k) = D_{ref}(k-1) - \Delta D$.

If $\Delta V < 0$, the voltage must be decreased further. The controller *increases* the reference duty cycle: $D_{ref}(k) = D_{ref}(k-1) + \Delta D$.

Negative Power Gradient **($\Delta P < 0$):** The previous perturbation moved the operating point away from the MPP. The algorithm must reverse the direction of the perturbation.

- If $\Delta V > 0$, the voltage was increased erroneously. The controller *increases* the reference duty cycle: $D_{ref}(k) = D_{ref}(k-1) + \Delta D$.
- f $\Delta V < 0$, the voltage was decreased erroneously. The controller *decreases* the reference duty cycle: $D_{ref}(k) = D_{ref}(k-1) - \Delta D$.

### *C. Step Size and Steady-State Considerations*

The perturbation step size, $\Delta D$, dictates the algorithm's transient response. While a large $\Delta D$ ensures rapid tracking during volatile irradiance conditions, it induces severe steady-state oscillations around the MPP, resulting in power dissipation. To mitigate this within the proposed architecture, $\Delta D$ is fixed at a conservatively small constant. Stability is preserved by executing this logic exclusively within the low-priority outer loop, shielding the fast inner-current loop from volatile duty cycle step changes.

## VII. MPPT IMPLEMENTATION FOR SOURCE SIDE TRACKING

While the generic P&O algorithm defines the mathematical logic for locating the MPP, its physical realization depends entirely on the nature of the converter's source-load interactions. As required by the specific constraints of this standalone generation system, the MPPT must operate

strictly as a source-side tracking mechanism, regulating the PV array regardless of the downstream load state.

*A. Source-Load Decoupling via Battery Clamping*

In the proposed topology, the 2-Phase Interleaved Boost Converter is interfaced directly with a battery bank. Unlike a purely resistive load where the output voltage fluctuates dynamically with load current, a battery acts as a massive capacitive sink. During standard charging phases, it effectively clamps the converter's output voltage ($V_{out}$) to the instantaneous battery voltage ($V_{bat}$).

Because $V_{out}$ is stiffly constrained by the battery's electrochemical state, the standard continuous conduction mode (CCM) voltage gain equation of the boost converter can be inverted to define the input voltage ($V_{in}$) from the perspective of the source:

$$V_{in} = V_{out} \cdot (1 - D) \approx V_{bat} \cdot (1 - D) \tag{28}$$

Equation (28) demonstrates that the solar PV array's operating terminal voltage ($V_{in}$) is directly dictated by the modulation of the duty cycle ($D$). Therefore, regulating $D$ through the P&O logic directly forces the PV array to operate at the specific voltage coordinate that yields maximum power extraction, effectively decoupling the source tracking from the battery's state of charge.

*B. Dynamic Impedance Matching*

From the perspective of the Maximum Power Transfer Theorem, the converter must actively match its equivalent input impedance ($R_{in}$) to the instantaneous internal resistance of the solar PV array ($R_{pv}$) at the MPP under varying environmental conditions. The input impedance of a boost converter connected to a clamped voltage load is defined as:

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{bat} \cdot (1-D)}{I_{in}} \tag{29}$$

By iteratively perturbing the reference duty cycle, the outer MPPT loop dynamically alters the apparent impedance $R_{in}$ presented to the solar panel. The algorithm reaches steady-state oscillation when $R_{in}$ successfully matches the optimal characteristic impedance of the array.

*C. Application to the Interleaved Topology*

In a standard single-phase boost converter, the MPPT algorithm directly drives the gate terminal of the MOSFET. However, in the proposed dual-loop system, the source-side tracking calculation is mathematically abstracted from the physical switching hardware. The P&O algorithm calculates a singular, global equivalent duty cycle required to achieve impedance matching.

This global value is passed exclusively to the shared $D_{ref}$ register. This abstraction allows the fast inner control loop to independently manage the 180° phase shifting and real-time current balancing required by the interleaved architecture without disrupting the overarching source-side voltage tracking mandated by the MPPT loop.

To evaluate the overall performance of the 2-phase interleaved boost converter, converter efficiency ($\eta$) is defined as the ratio of total output power ($P_{out}$) delivered to the load to the total input power ($P_{in}$) drawn from the source:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \times 100\%$$

where $P_{loss}$ represents the aggregate cumulative power losses incurred across the power stage components. For a high-frequency interleaved topology operating in Continuous Conduction Mode (CCM), total losses are primarily categorized into semiconductor conduction losses ($P_{cond}$), switching losses ($P_{sw}$) in the MOSFETs, diode recovery losses, and winding/core losses in the toroidal inductors ($P_L$).

The output power is expressed in terms of average load voltage ($V_{out}$) and load current ($I_{out}$):

$$P_{out} = V_{out} \cdot I_{out}$$

MOSFET conduction losses are governed by the root-mean-square (RMS) branch currents and the drain-source on-state resistance ($R_{DS(on)}$). Because the input current is split symmetrically across the two parallel phases, the RMS current per branch is significantly reduced compared to a single-phase topology, directly mitigating thermal dissipation:

$$P_{cond,MOSFET} = I_{L,rms}^2 \cdot R_{DS(on)} \cdot D$$

where $D$ represents the converter duty cycle. Furthermore, the interleaving technique ensures that the high-frequency ripple components partially cancel out at the input and output nodes, minimizing RMS current stress on the filter capacitors and maximizing overall conversion efficiency.

## VIII. MATLAB SIMULATION RESULTS

Prior to integrating the time-domain decoupled control logic, it is critical to validate the foundational power stage of the 2-Phase Interleaved Boost Converter. To analyze the baseline switching dynamics, current sharing capabilities, and Continuous Conduction Mode (CCM) stability, an open-loop plant model was developed using the MATLAB/Simulink (Simscape Electrical) environment.

*A. Open-Loop Plant Model Validation*

The simulation model was constructed to evaluate the pure hardware response of the interleaved topology. An ideal DC voltage source was utilized at the input to provide a stable testing baseline, removing the non-linear complexities of a PV array for this stage of validation. The two parallel phases were modeled using discrete series RLC branches for the inductors ($L_1$, $L_2$), interfaced with ideal MOSFET and diode blocks.

To simulate the foundational interleaving mechanism without the overarching STM32 controller, two independent Pulse Generator blocks were deployed. These generators were configured to operate at a fixed duty cycle with a strict 180° phase shift, driving the MOSFET gate terminals. The system was loaded with a standard resistive branch to evaluate the output power flow.

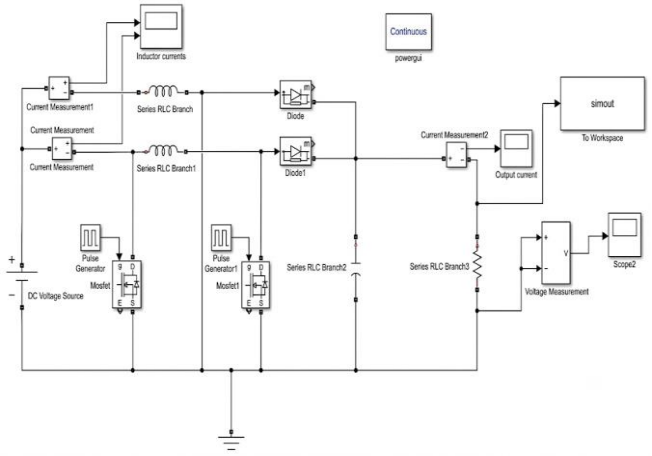


**Fig. 5.** MATLAB/Simulink of the 2-Phase Interleaved Boost Converter.

*B. Inductor Current Analysis and CCM Verification*

A primary objective of the simulation was to confirm that the selected passive component values successfully maintain Continuous Conduction Mode (CCM) under steady-state operation. Fig. 6 illustrates the simulated transient response of the inductor currents.

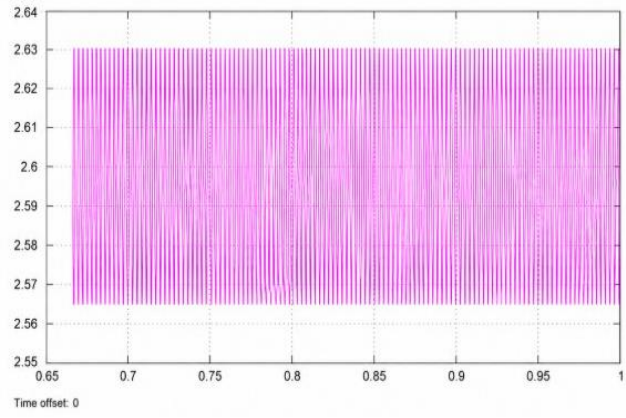


**Fig. 6.** Simulated steady-state inductor current waveforms demonstrating CCM operation.

The scope output demonstrates a highly stable, continuous current profile. The inductor current oscillates between a minimum boundary of approximately 2.557 A and a peak of 2.632 A. The absence of the current dropping to zero during the switching cycle definitively verifies that the converter operates strictly within CCM. Furthermore, the tightly grouped high-frequency ripple confirms that the parallel branches are sharing the input current load symmetrically, validating the baseline physical design before the introduction of the PI current-balancing control loop.

This symmetrical distribution inherently halves the thermal stress on the individual semiconductor switches and magnetic components, significantly enhancing the overall reliability of the power stage. Additionally, the sustained CCM operation directly validates the theoretical sizing of the 330 muH phase inductors for the designated 50 kHz switching frequency. By establishing such a robust and naturally balanced open-loop plant, the system inherently minimizes input-current harmonics, providing an optimal, low-noise foundation for maximum power extraction from the photovoltaic source.

*C. Output Current Characteristics*

The efficacy of the 180° phase-shifted pulse generation is most evident in the output characteristics of the converter.

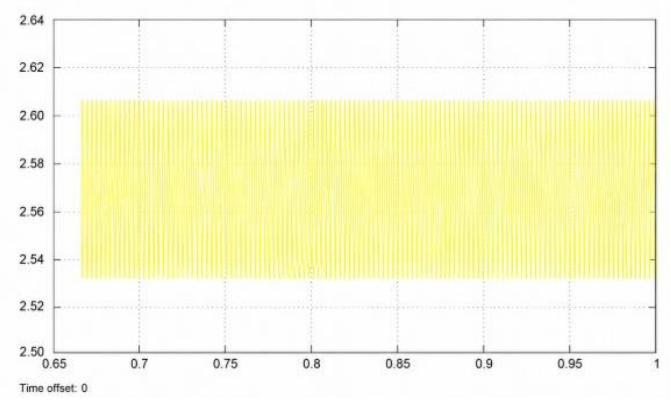


**Fig. 7.** Simulated output current waveform of the interleaved converter.

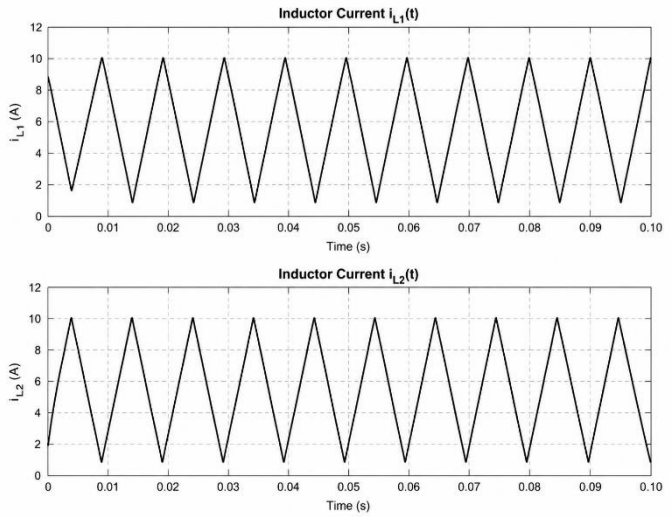


**Fig. 8.** Inductor currents ($i_{L1}$ and $i_{L2}$) illustrating phase-shifted operation and ripple current cancellation in the proposed IBC.

As shown in Fig. 7, the output current waveform maintains a steady average of approximately 2.565 A, fluctuating between 2.518 A and 2.613 A. The high-frequency ripple observed in the output stage is a direct result of the overlapping conduction cycles of the two phases. In a single-phase converter, this ripple magnitude would be significantly higher; however, the simulation proves that the interleaved topology successfully facilitates ripple cancellation, thereby reducing the stress on the output filter capacitor and delivering a smoother power profile to the load.

*D. Hardware Design and Component Selection*

The physical architecture of the experimental 2-phase interleaved boost converter prototype is systematically categorized into power conversion, high-speed gate drive, filtering, and real-time sensing stages.

The main high-frequency power conversion stage utilizes two N-channel IRF460 power MOSFETs (rated at 500V and 20A) as the primary switching elements for Phase 1 and Phase 2. To ensure rapid transition times and minimize dynamic switching losses, these devices are driven by independent IR2110 high-speed gate driver ICs. Each driver incorporates a dedicated bootstrap network consisting of a 10 µF capacitor and a UF4007 fast-recovery diode. High-frequency output rectification per phase is handled by BYM36D fast-recovery diodes, complemented by ultra-fast UF5408 diodes configured for freewheeling and snubber protection to suppress voltage spikes.

Energy storage and continuous conduction mode (CCM) operation are maintained by custom hand-wound toroidal inductors. These inductors are wound using thick 18 AWG copper wire to efficiently handle peak branch currents without core saturation. At the output stage, a parallel bank of four 100 µF, 63V electrolytic capacitors is implemented to minimize equivalent series resistance (ESR) and suppress high-frequency output voltage ripple.

For closed-loop telemetry and control coordination, the sensing subsystem is divided into input and output measurement blocks. Real-time input power parameters ($V_{in}$ and $I_{in}$) are captured at the source stage using an INA219 digital power monitor communicating via an $I^2C$ bus. On the output side, a high-precision voltage divider scales the elevated DC bus voltage down to a 0–3.3V range, making it fully compatible with the analog-to-digital converter (ADC1) peripheral of the microcontroller. Concurrently, output current ($I_{out}$) tracking is achieved via a low-side 0.1 Ω shunt resistor paired with an INA180 current sense amplifier, which routes a proportional analog voltage signal to the ADC2 peripheral for real-time monitoring and feedback processing.

## IX. CONCLUSION

This paper has presented the foundational design, theoretical control architecture, and simulation-based validation of a 2-Phase Interleaved Boost Converter intended for standalone renewable energy integration. To address the inherent computational conflict between slow source-side Maximum Power Point Tracking (MPPT) and high-speed phase current regulation, a time-domain decoupled dual-loop control strategy utilizing an STM32 microcontroller was proposed. Prior to physical closed-loop implementation, the fundamental power stage was rigorously evaluated using an open-loop MATLAB/Simulink plant model. The simulation results successfully validated the mechanics of the interleaved topology. The inductor waveforms confirmed stable Continuous Conduction Mode (CCM) operation and symmetrical current distribution across the parallel branches. Furthermore, the application of 180° phase-shifted pulse generation yielded a definitive reduction in output current ripple, verifying the architectural advantages of interleaving for minimizing stress on DC-link capacitors and battery loads.

Ultimately, the established open-loop stability provides a highly reliable, validated plant model. This foundational hardware verification successfully paves the way for the future physical integration of the proposed discrete-time PI current controllers and the decoupled P&O MPPT algorithm in a complete hardware prototype.

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