Advanced PLL Readout Design Using MEMS Technology for Implantable Cardiac Monitoring Systems.

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ABSTRACT

A MEMS-based implantable Phase-Locked Loop (PLL) readoutsystemisdevelopedtomonitorheartfunctionafter transplantationinacontinuousandefficientmanner.Inthis system, a MEMS sensor is used to detect small cardiac vibrations that represent the heartbeat and overall activity ofthetransplantedheart.Sincethesesignalsareveryweak, they are processed using a PLL circuit designed with CMOS technology at 45nm and 90nm, which helps in stabilizing and converting the signals into accurate frequency outputs for proper analysis. The design mainly focuses on achieving low power consumption, which is important for implantable devices to ensure longer battery life, along with high-speed operation for real-time monitoring.Itisalsodesignedtobecompactinsizesothat itcanbeeasilyimplantedinsidethehumanbody.Important parameters like area, delay, and power are optimized to improve the overall performance of the system. By using advanced CMOS technology, the system becomes more efficientandreliable.Thissystemenablescontinuousreal-time monitoring of the transplanted heart, reducing the needforfrequenthospitalvisitsandinvasivefollow-ups.It also helps in early detection of any abnormalities, thereby improving patient safety. Simulation results show that the system performs effectively and provides reliable output under different conditions. Overall, this work combines MEMSsensorsandVLSIdesigntocontributetoadvanced healthcare solutions by providing a smart, compact, and lessinvasiveheartmonitoringsystem.Thissystemhas the potential to play a significant role in future implantable medical technologies and personalized healthcare monitoring..

GeneralTerms

VLSI Design, Low-Power Circuits, Implantable Systems, Signal Processing, MEMS Sensors.

Keywords

Implantable heart monitoring readout circuit, MEMS readout, PLL(phase locked loop), VCO(voltage control oscillator), sensor's, CMOS technology.

1. INTRODUCTION

Heart transplantation is one of the wonders of modern medical science. For patientswith end- stage heart failure, heart transplantation is often life-saving and offers fresh opportunities for living when all other medical treatments have failed. While it is a very effective surgical intervention, long-term graft survival depends on continuousmonitoringaftertransplant.Hence,whenoneis given a new heart, it is essential to ensure that the transplanted organ functionswell, adaptsto thehostbody, and does not suffer from rejection or other complications.

Continuous monitoring by physicians enables them to assess the performance of the transplanted heart and provides an early indication of abnormal conditions thatmayarise.Thisfollow-upcareenablesthedetectionof complications like arrhythmia, rejection, and cardiac insufficiency before they become critical. Good post-transplantcarenotonly enhancesthequality oflifefor the recipient but also minimizes the risks of organ failure, hospital re- admissions, and medical emergencies.

Overthepastfewyears,technologicalinnovation has struck medical electronics, especially within implantable biomedical systems. The MEMS and CMOS technologieshaveplayed vitalroles in thedevelopment of implantable monitoring devices. MEMS refers to a microsystem that integrates the mechanical and electrical components on one chip. Due to the compact size, high sensitivity, low power consumption and the ability to functionwithinmicro-scaleenvironments,theyarehighly suitable for biomedical applications.

IntegrationofMEMSwith CMOScircuitsmakes the system efficient, intelligent and more reliable. For this reason, CMOS technology has advantages of a low power requirement, high noise immunity and scalability, thus allowing the design of compact circuits with extremely strong signalprocessing capabilities.MEMScoupled with CMOSformsapromisingcombinationtowardsdeveloping measuringcertainphysiologicalparameterssuchasheart rate, blood pressure and electrical activity within the human body continuously.

A MEMS-based implantable system provides a feasible solution for these challenges. MEMS sensors, which can detect very minute mechanical changes such asvibration,displacement,oralterationofpressure,have a direct relationship with heart activity. When these sensors are integrated with CMOS circuits for signal processing, they provide real-time information on the performanceofthetransplantedheart.Theacquireddata can be analyzed by health professionals for quick and informed clinical decisions. Systems of this sort are extremelyimportantinordertoensuretheearlydetection of potential complications that may help achieve much better survival rates for patients after transplantation.

AnothermajorbenefitofintegratingMEMSwith CMOStechnologyistheenergyefficiencyofthedesign. Since such implantable devices need to work for a long timeinsidethebody,theirpowerconsumptionshouldbe as low as possible. CMOS-based circuits facilitate this with low operating voltages and very low current consumptions, thus allowing for extended life of the power source with reduced heating effects. This ultimately makes the system safe and suitable for long-term biomedical implantation.

Besides, miniaturization of electronic components allows creating compact, lightweight, and biocompatible implants. These can be easily placed inside the patient's body without discomfort, continuously acquiring physiological data while maintaining communication with external monitoring equipment. The result is a seamless and efficient health-trackingsystemthatsupportsbothpatientsanddoctorsin managingpost-transplantcare.Thiswillbringuptheidea of a MEMS-based PLL readout system using CMOS technology because of this increasing demand for accurate and reliable post-transplant monitoring. PLL is usually applied to lock and stabilize signal frequencies. In biomedical applications where the accuracy and stabilityofthesignalareimportant,thiscircuitcanbeof great use. Implementing PLL techniques in readout circuitries can minimize noise and allow for a more accurate capture of the heart's electrical signals. This enables more dependable to analysis of cardiac performance, helping medical professionals detect even minor deviations in heart function.

On one hand, the integration of MEMS sensors withCMOStechnologyforhearttransplantmonitoringisa huge step toward intelligent biomedical systems. Such systemscould be able to continuously render performance feedback of the transplanted heart in real time, therefore reducing the chances of complications. A MEMS-based PLL readout system plays an important role in achieving efficient, compact, low-power monitoring, and is thus an ideal solution for implantable biomedical applications.

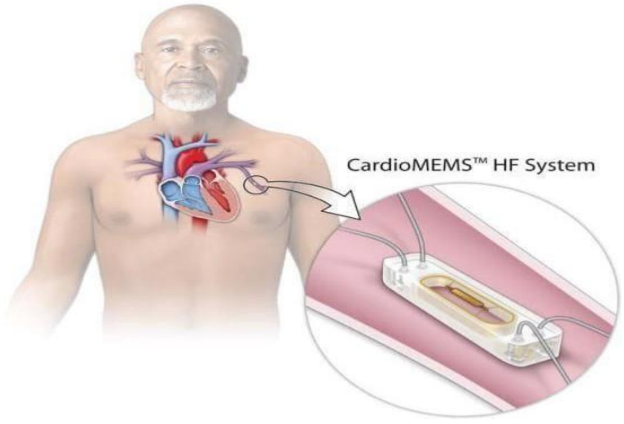


Figure1:MEMSSensor

2. CircuitDesigninCadenceVirtuoso

Oncethetechnologynodesareselected,thenextstepisthe circuit design stage using Cadence Virtuoso Schematic Editor.Inthisstage,theoverallPhase-LockedLoop(PLL) systemisdevelopedbydesigningitsimportantsub-circuits with proper attention to accuracy and performance. The design is carried out at the transistor level, which helps in achieving precise control over the circuit behavior and ensuresreliablefunctionality.Eachcomponentiscarefully simulated and analyzed to verify its operation under different conditions. The main aim of this stage is to optimize important parameters such as delay, power consumption, and stability, which are very important for implantable biomedical applications. By using advanced CMOStechnology,thecircuitsaremadecompact,efficient, and suitable for real-time monitoring systems. This step playsa crucialrolein ensuring that the PLL system works effectively and meets the required design specifications.

- DelayCell,BiasingCircuit,andComparatorCircuitare designed and simulated.
- Eachcircuitisexcecutedatthetransistorlevel,ensuring functionalityand accuracy.
- The Delay Cell is designed to control the oscillation frequency and phase characteristics, which are vital for synchronization.

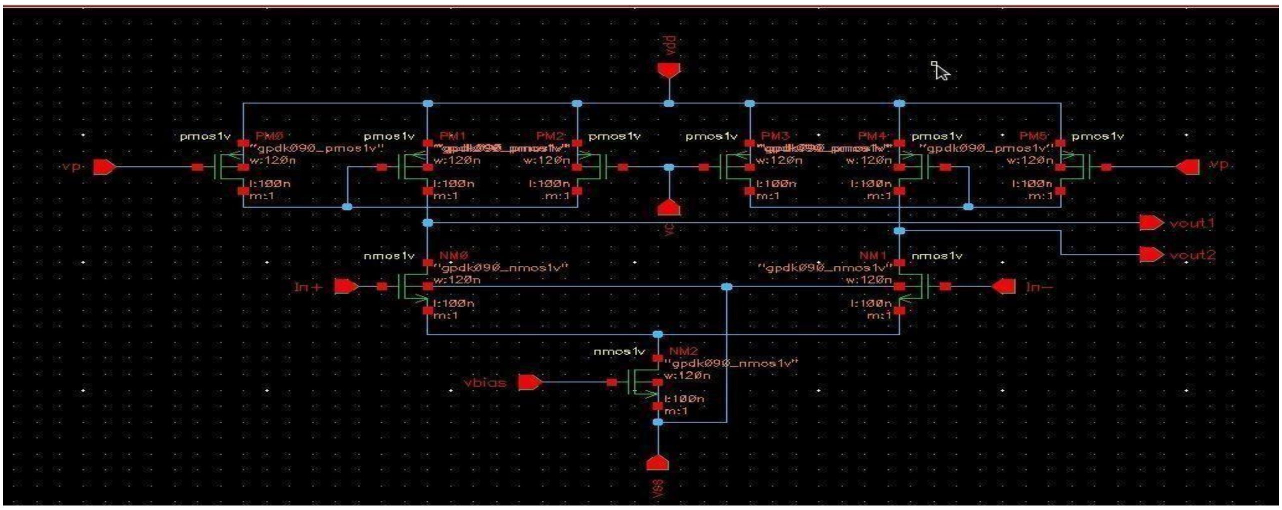


Figure2: Delaycellcircuit

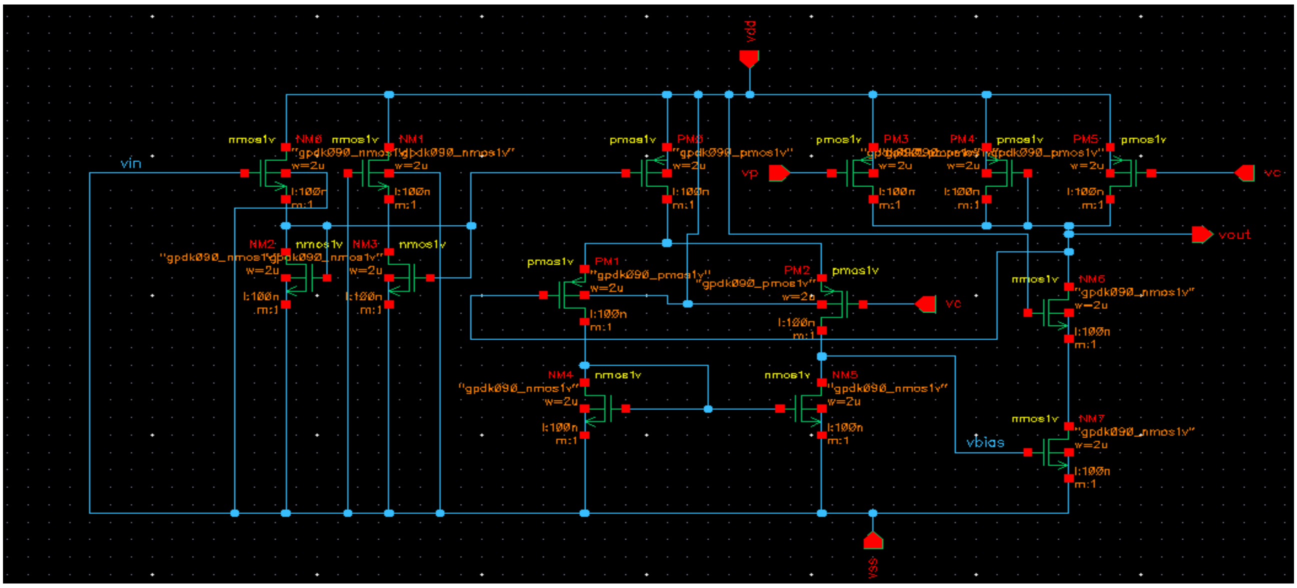


Figure3:BiasingCircuit

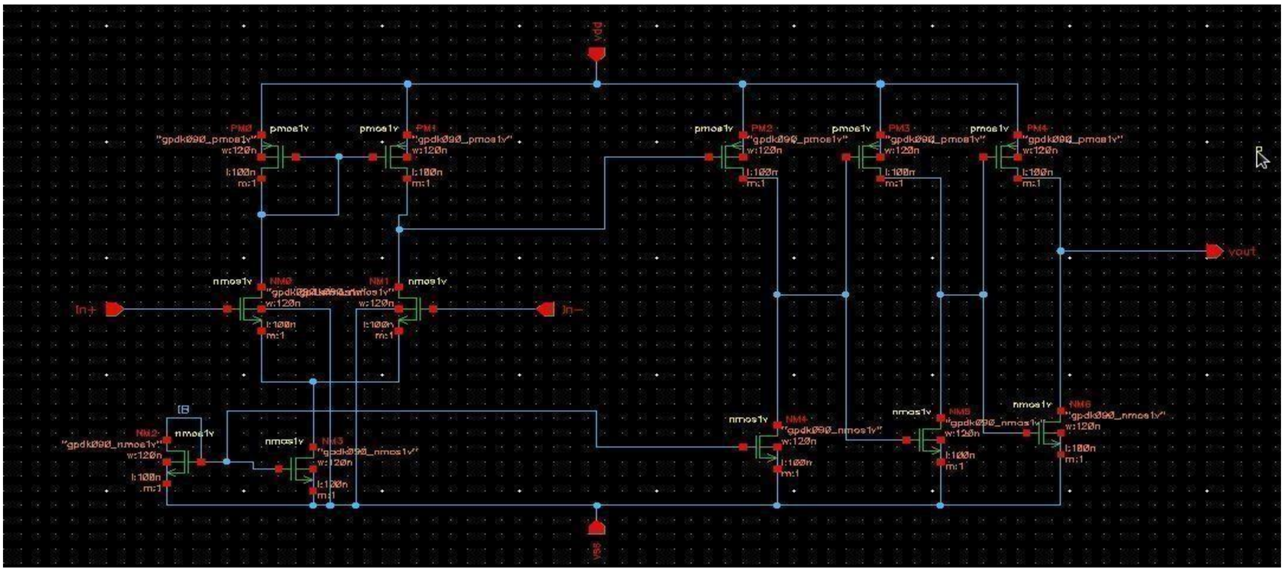


Figure4:ComparatorCircuit

TheCadenceVirtuosoenvironmentwasemployedforits design, which includes schematic capture, choosing devices from the technology library, and their interconnection.Eachtransistor,resistor,andcapacitoris chosen based on its characteristics, as defined in the respective 45 nm and 90 nm PDK. Once the schematics have been drawn, the circuits undergo simulation by Cadence Spectre Simulator, which gives a detailed waveform analysis of key electrical parameters such as voltage levels, propagation delay, current consumption, and power dissipation. Several test benches are realized for each circuit in order to verify the correctness of its behavior before passing to the layout phase.

3. LayoutDesign

Once the schematic simulations show satisfying results, the next step is LayoutDesign. The layout for the Delay Cell and other important circuits is drawn using the CadenceVirtuosoLayoutEditor.Alayoutdesignshows theactualphysicalrepresentationofacircuitwithhowit would look when fabricated on a chip. It includes transistor placements, metal interconnections, vias, and layersnecessaryforbothdiffusionandpolysilicon.Extra attention must be paid to the design rules given by the foundry on the selected technology node.

This phase is important because it bridges the gap between the circuit level design and its physical implementation.Awell-designedlayoutensuresthatthe resultant circuitwillbe fabricated with minimum errors. The layout also helps in estimating total area, parasitic capacitances, and interconnect delays that may slightly affect performance compared

DRCandLVSVerification

The DRC makes sure that the layout is according to all geometrical and process-related rules defined in a technology file. These include minimum spacing, width of metal layers, via placements, and overlap constraints. AlltheDRCviolationsfoundarecorrectedonthespotto keep fabrication problems at a minimum.

LVS verification provides assurance that the electrical interconnections in the layout are exactly as described in the schematic. It checks the netlist of the layout against the schematic netlist and ensures consistency between all parts and their respective interconnections. If LVS is completed successfully, it means that the physical layout accurately represents the designed circuit.

4. ComparisonwithExistingPaperResults

After the verification stage, the simulated results are analyzed and compared with existing research papers related to PLL and biomedical readout designs. The key parameters evaluated include delay, power, area, and noise performance for both 45 nm and 90 nm. This comparative analysis validates the proposed design’saccuracyandhighlightsimprovementsachieved intermsofenergyefficiencyandsignalperformance.The obtained results show that as the technology node scales down to 45 nm, power consumption and area decrease, while the speed and frequency response improve. However, a slight increase in noise level (SNR degradation) is observed due to higher leakage and smallerdevicegeometry.Inthisway,theworkillustrates that, by comparison, the 45 nm node yields superior general performance of implantable biomedical circuits in low-power, compact, and high-speed applications. This further justifies that the suggested design methodology is effective and agrees well with the previously reported trend in CMOS scaling.

Based on performed simulation and analysis, it is concluded that the 45 nm CMOS technology provides betteroverallperformancecomparedto90nmbecauseof reducedpower,smallerarea,andfasterresponse,though ithasslightlyhighernoise.Theseareacceptabletradeoffs for biomedical monitoring systems, where power efficiency and size reduction are primary design goals.

The methodology followed in this work is well-organized, going through problem identification and technology selection, design, layout, verification, and performance comparison in a very systematic way. This project has designed MEMS-based PLL readout system that has proven to be efficient, stable, and suitable for implantable biomedical applications. It achieves the objectives of low power consumption and reduced area while ensuring reliable signal monitoring; hence, it can beapotentialcandidateforfutureintegrationinreal-time heart transplantation monitoring systems.

To compare the performance of 45 nm and 90 nm technologies and identify the most efficient one for biomedical applications. This project responds to the increasing demand for continuous and reliable patient monitoring systems, especially in the case of heart transplantation. Classical monitoring devices are bulky, high-power devices that are not suitable for long-term implantation inside the human body. Providing compactness, low power, and a high degree of accuracy are in great demand for biomedical circuits. While MEMS-based sensors can detect physiological parameterswithhighsensitivity,theydoneedanefficient readout system that is able to process and transmit the sensed signal accurately. In this respect, a CMOS-based PLL circuit has shown high precision in frequency synchronization and has given stable signal conversion, whichmakesitidealforbiomedicalreadoutapplications. IntegratingMEMSsensorswithCMOSPLLtechnology, this project aims at developing miniaturized and energy- efficient implantable the a systems capable of continuously monitoring cardiac signals to assure performance, reliability, and post-transplant care. Ultimately, this project is driven by the goal of contributing to advanced healthcare technology through the development of intelligent, implantable biomedical systems.

Softwarerequirements

The domain of Very Large-Scale Integration design is complex,intriguing,andturnsideasintothebasicsilicon components of today's electronics. Behind this change, there are numerous powerful tools that make the design processes possible. One of these tools is Cadence; it is a leading name in Electronic Design Automation and contributes significantly to VLSI design.

CadenceDesignSystemsplaysaveryimportantrole in providing a widerangeof tool suites that simplify the complex process of integrated circuit design. Due to the advancementinVLSItechnology,theimportanceofthese tools increases in order to make designs efficient, accurate, and innovative. This blog post examines the essential Cadence tools for VLSI design, emphasizing theirfeatures,applications,andadvantagesforengineers and designers

5. CadenceVirtuosoPlatform

TheCadenceVirtuosoPlatform isanend-to-endanalog, mixed-signal, and custom digital design platform. This all-encompassing suite provides various design tasks, right from schematic capture to physical design and verification. This Tool is ideal for VLSI Design. The CadenceVirtuosoPlatformrepresentstheindustry'smost comprehensive tool suite for custom integrated circuit design, widely utilized in analog, mixed-signal, RF, and custom digital design applications. It offers a totally integrated environment that allows schematic capture, layoutediting,simulation,andverification-startingfrom a common database-thereby making it an indispensable tool in every semiconductor company and research institute.

At the heartof theplatform, Virtuoso Schematic Editor offers hierarchical circuit design while maintaining accuracy and efficiency. It includes electrical rule checking and supports integration with SPICE-based simulation tools like Cadence Spectre, enablingsmoothcircuitvalidation.TheVirtuosoLayout Suite provides comprehensive features for manual and automated physical design creation: constraint-driven design, shape-basedrouting,and advancednodesupport for FinFET and nanoscale technologies in L, XL, and GXL editions, respectively. Virtuoso ADE Suite enhances themulti-modesimulation, statisticalanalysis, and waveform visualization of the platform in order for designers to optimize performance and reliability.

Key advantages with Virtuoso include deep integrations with other Cadence products like Virtuoso Multi-Mode Simulation for fast and accurate circuit simulation, Assura and Pegasus for Design Rule Checking and Layout vs. Schematic, and Quantus for parasitic extraction.

The platform also integrates seamlessly with Cadence Innovus for digital implementation, hence enabling mixed-signal designs in an efficient way. Support for Process Design Kits from major semiconductor foundries ensures that modeling of real-world manufacturing constraints is accurately captured.

Virtuoso has extensive use in high-performance analog circuits, RF transceivers, data converters, power management ICs, sensor interfaces, and custom memories. It represents an enabling environment for doingadvancedmixed-signaldesigninwhichanalogand digitalcomponentsinteractintimately.CadenceVirtuoso delivers automation, AI-driven optimizations, and collaborative design capabilities to engineers; it enables highly optimized and manufacturable IC designs while reducing the time and cost of development.

FeaturesandApplications

- **Virtuoso Schematic Editor:** Enables intuitive, productiveschematicentryandeasymodification of designs.
- **Virtuoso Layout Suite:** Its impressive layout functionality allows users to set up custom, analog, and RF designswith automation features tofacilitate expedient layout.
- **Virtuoso Analog Design Environment:** Provides feature-rich simulation and analysis capabilities that help designers to first validate their design by thorough testing.

Benefits

- Streamlinesthedesignprocessusingintegratedtools.
- Improvesproductivitywithautomationandadvanced design features.
- Ensuresdesignaccuracythroughcomprehensive simulation and analysis.

6. CadenceSpectreSimulationPlatform

The Spectre Simulation Platform is an extremely powerful tool in analog and mixed-signal simulation, acclaimed for its accuracy and performances. Cadence Spectre Simulation provides a high performance, industry-leading circuit simulator, widely used in the design ofanalog,mixedsignal,RFand custom digital.It provides a comprehensive set of simulation engines, comprising Spectre APSSpectre XSpectre RFand the a

SpectreAMS,whichallowdesignerstoanalyzethe behavior of circuits with high accuracy and efficiency.

It provides Multi Mode simulation capabilities, including DC, AC, transient, noise, and Monte Carlo analysis, for the most exhaustive verification in a wide range of operating conditions. Spectre integrates seamlessly into the Cadence Virtuoso design in Environmentforefficientschematicindrivensimulation workflows. It also supports Process Design Kits from majorsemiconductorfoundriestoensurehighlyaccurate modeling of real manufacturing effects. Advanced features include high-speed matrix solvers, parallelization for multi-core processing, and AI-driven optimizationstoenablefasterconvergenceandimproved simulation speed in complex circuits. Spectre is widely utilized in applications such as high-speed data converters,powermanagementICs,andmemorydesigns, placingitasanimportanttoolamong engineers working with state-of-the-art semiconductor technologies.

FeaturesandApplications

- **Spectre Circuit Simulator:** Provides accurate SPICE-level simulation for a wide range of circuits, from analog to RF.
- **Spectre X Simulator:** Offers high performance simulation for large and complex designs, and shortens the verification cycles verification cycles.
- **Spectre RF:** Offers special simulation features tailoredforRFandmicrowave circuits.

Benefits

- Guarantees dependable and accurate simulation results.
- Accelerates the verification process through high-performance simulation engines.
- Accommodatesa wide variety of application areas, rangingfromsimpleanalogcircuitstohighlycomplex RF designs.

7. Implementation

i. Project&TechnologySetup

First, launch Virtuoso by using virtuoso &, which opens the Library Manager. Then go to File → New → Library, give a name to the library (for example, delay_90), and attach it to an existing technology. After that, choose GPDK90(oryourrequiredtechnologynode)andclickOK. Next, go to File → New → CellView. In this step, select your library, give the cell name such as Delaycell, choose the required view like layout for backend implementation or schematic if it is already done, select the tool as Virtuoso, and then click OK.

ii. SchematicDesign

Open the Library Manager, then go to File → New → CellView and select your created library. Enter the Cell Nameasinverterandchoosethe Viewasschematic,then click OK. Next, go to Place → Instance and browse the library (for example, analogLib). Add the required components such as pmos transistor, nmos transistor, vdd,gnd,andvpulse.Afterplacingthecomponents,wire alltheterminalsproperlysuchthatthegateofPMOSand NMOS is connected to the input, the PMOS source is connected to VDD, and the NMOS source is connected to GND. The drains are shorted together to form the output.ThenchecktheDCvoltageas1.8Vandlabelthe pinsasIN,OUT,VDD,andVSS.Finally,performCheck and Save for the schematic.

iii. SymbolCreation

With schematic open,go to Create→Cellview →From Cellview and select From View as schematic and To Viewassymbol,thenpressOK.Thesymboleditoropens where you need to draw the symbol box and place the required pins. After that, name the symbol as Inverter SymbolandclickOK.Finally,saveandclosethesymbol editor.

iv. TestSchematic(SimulationSetup)

Createanewcellandnameittest_delay_cell.Thengoto Place→Instance andadd thesymboloftheinverterthat you have created. Next, add a VDC source of 1.8 V for thesupply.AlsoaddaVPULSEfortheinputsignalwith parameterssetasVoltage1=0V,Voltage2=1.8V,Rise time=10ns,Falltime=10ns,Period=40ns,andWidth = 20 ns. After that, connect the output node to a probe. Finally, perform Check and Save.

v. SimulationUsingCadenceSpectre

Launch ADE L or XL (Analog Design Environment), thengotoSetup→ModelLibrariesandbrowsetoselect gpdk90.scs and add it. After that, go to Setup → Environment and select the analysis view as schematic. Next, go to Analyses → Choose and select Transient (tran) analysis, set the stop time as 100 ns according to the pulse, and click OK. Then go to Outputs → To be Plotted → Select on Schematic and choose both input (IN) and output (OUT). After that, perform Netlist and Run to start the Spectre simulation. Once the simulation iscompleted,theoutputwaveformswillopeninVirtuoso Visualization (ViVA), where the input can be observed as a square pulse and the output will appear as an inverted waveform.

vi. OpenLayout &DefinePRBoundary

Inlayoutview,pressShift+F1todisplaythelayerpalette. Then create the PR boundary by selecting the pr bound

Boundary layer (or Boundary) and draw a rectangle that is large enough to accommodate all devices and routing. Make sure that all devices and pins will touch this boundary, as it is required for DRC, and you can adjust the exact size using Q (properties). Also, note down the Width ×Height of the boundary to calculate the area. Next, place the devices by going to Create→Instance (i) and selecting pmos1v and nmos1v PCells from the technology library. Place the PMOS in the n-well region, which is usually handled automatically by the tool, and set the Body Type as Integrated so that the body is tied to the well. Then place the NMOS in the p-substrate region. While placing, maintain proper orientation of source and drain as per your design style, and ensure that the gate polys are aligned properly so that shorting becomes easy. After placing the devices, check the wells, contacts, and pins. Ensure that the PMOS is fully inside the n-well and extend the n-well if needed so that there are no gaps. Add body ties by placing p+ tap for the substrate and n+ tap for the n-well, and connect them to VSS and VDD respectively. Finally, place the pins carefully, making sure that all pins touch the PR boundary; for example, place the VDD pin at the top edge using metal1 and create it using Apply→High/Pin option. Place the VSS pin along the bottom edge using metal1, ensuring it properly aligns with the overall layout structure and touches the PR boundary as required. Then, position the IN and OUT pins along the left and right edges respectively, also using metal1 so that routing becomes simple and consistent. While creating these pins, go to Create → Pin and select the metal1 layer for all routing pins. Carefully assign the correct direction for each pin, such as input for IN, output for OUT, and power for VDD and VSS. Make sure all pins are clearly placed, properly labeled, and connected in a clean and organized manner so that the layout is easy to understand and meets design rules.

For the gate and device connections, begin by joining the polysilicon gates of both the PMOS and NMOS transistors using Create→Path and selecting the poly layer, ensuring a proper and continuous connection so that both devices receive the same input signal. This alignment is important because it directly affects the switching behaviour of the inverter. After connecting the gates, proceed to connect the drains of both transistors together using a metal1 path, which forms the output node (OUT). Make sure this connection is clean and properly aligned to avoid unnecessary bends or overlaps. Then connect the source of the PMOS transistor to VDD and the source of the NMOS transistor to VSS using metal1 routing, ensuring that the power and ground connections are strong and clearly defined. Wherever there is a transition between layers, such as from polysilicon to metal1 or from metal1 to metal2, use Create→Via and select the correct via type like poly_m1 or m1_m2 by right-clicking. Place these vias carefully with proper spacing from edges to satisfy enclosure rules and avoid DRC violations. Proper via placement very important for reliable electrical connectivity between layers.

After completing the basic connections, move on to finishing the routing and performing layout cleanup. Follow the minimum width and spacing rules specified by the technology to ensure that the design is manufacturable. Try to keep all routing paths straight, short, and orthogonal (horizontal or vertical) instead of using unnecessary angles, as this improves readability and reduces potential errors. Check that all devices, contacts, and pins are properly aligned and that each one touches the PR boundary, which is a mandatory requirement for DRC. If any element is not aligned correctly, use the move command (m) to adjust its position carefully. Also, regularly perform Check and Save during this process so that any small mistakes can be identified and corrected early, preventing bigger issues later in the design flow.

Once the layout is properly completed, the next step is to run the Design Rule Check (DRC) using Assura. Go to Assura → Run DRC and ensure that the Technology Path is correctly set; if it appears blank, browse and select the GPDK90 technology directory, which usually needs to be configured only once. Provide a suitable name for the run, such as drc1, and start the process. After the run is complete, carefully examine all reported errors and warnings. These may include spacing violations, missing contacts, or improper overlaps. Each error must be fixed one by one to make sure the layout fully satisfies all design rules required for fabrication. Running DRC multiple times after corrections is a good practice to ensure that no violations remain.

Following DRC, perform Layout versus Schematic (LVS) verification using Assura→Run LVS. In this step, select the schematic view as the reference and the current layout as the comparison view. Assign a run name like lvs1 and execute the LVS check. This process verifies whether the layout exactly matches the intended schematic design. If mismatches occur, they may be due to issues such as missing connections, incorrect pin names, improper body ties, or wrong transistor dimensions. Carefully debug these errors and make the necessary corrections in the layout. Repeat the LVS process until the result shows LVS PASSED, which confirms that the layout is electrically equivalent to the schematic and is ready for further steps.

Finally, measure the area of the layout for documentation and analysis purposes. Select the PR boundary rectangle and press Q to open the properties window, where the Width and Height values will be displayed in micrometers. Use these values to calculate the total area using the formula Area = Width × Height in µm². Record this calculated area in your results table for reporting. In some cases, the tool itself may directly display the area in the properties section, which can also be noted. Accurate area measurement is important for an comparing designefficiency andoptimizing layoutsizein VLSI design.

8. TestSchematic&DC responseofBiasingcircuit

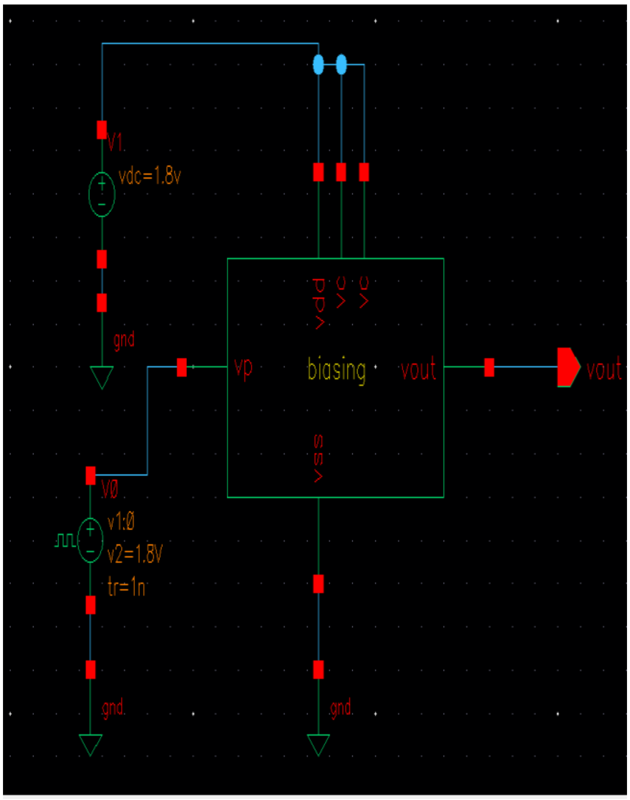


Figure5:TestschematicofBiasingCircuit

The biasing circuit is a very important block in the entire systemsinceitprovidesstable DC operating conditions to allothersub-circuitssuchasthedelaycellandcomparator. The primary duty of the biasing block involves creating fixed DC voltages-namely, VP, VC, and Vbias-to ensure proper operation of the circuit in its right region without anyfluctuationswhatsoever.Thebiascircuitcontrolsboth thecurrentandvoltagelevelsinthePLLreadoutsystem,a very significant component in attaining consistent performance. If the bias is unstable, the entire circuit may shiftitsoperatingpointandcausevariationsindelay,gain, ornoise.Therefore,thebiasingblockactsasthe“heart”of the analog system and keeps everytransistor in the proper operating region.

In this design, the DC response of the biasing circuit clearly shows how the output behaves with respect totheinputvoltage,andithelpsusunderstandthestability and working region of the circuit in a very practical way. Atthebeginning,whentheinputvoltageisverysmall,the outputofthebiasingnetworkremainsalmostconstantand flat.Thishappensbecausethetransistorsinsidethebiasing circuit are not fully turned ON yet; they are either in the weak conduction region or close to cutoff. In this region, only a very small current flows, to the circuit. Because of this, the output voltage remains stable and doesnotfluctuate,whichisactuallyagoodsign.Itshows that the biasing circuit is strong enough to ignore minor variations in input and maintain a steady output. This kindofstableregionisveryimportantbecauseitensures that the circuit does not get affected by noise or small disturbances.

As the input voltage slowly increases and reaches a certain level called the threshold voltage, the behaviourofthecircuitstartstochange.Atthispoint,the transistors begin to conduct properly and move into the strong conduction or saturation region. Once this happens, the output no longer remains flat. Instead, it suddenly starts to rise or drop depending on the circuit design. This sharp change indicates that the biasing circuit has entered its active operating region where the current becomes well-defined and controlled. This transition is very important because it marks the point where the circuit becomes fully functional and starts responding effectively.

The significance of this behaviour is very meaningful in the overall design. The initial flat region proves that the biasing circuit can maintain a constant output voltage, which is necessary for controlling the delay in circuitslike thedelaycell. A stable biasensures that the delay remains predictable and does not vary randomly. Then, the point where the output changes rapidly represents the designed operating point of the circuit. This is where the circuit is expected to work in a proper and controlled manner. The DC response, therefore,confirmsthatthebiasing blockisstableovera wide range of input voltages and only changes when it reaches its intended threshold region.

In addition to this, the biasing circuit plays a keyroleinsupplyingstableDCvoltagessuchasVP,VC, and Vbias to other important blocks like the delay cell and comparator. These voltages are very important becausetheycontrolthecurrentandvoltagelevelsinside thecircuit.Ifthesevaluesarenotstable,theentiresystem canshowfluctuationsandgiveinaccurateresults.Theuse of a cascaded 2T voltage reference in this design makes this even more effective. Here, two transistors are connected in such a way that they generate a fixed reference voltage. This structure helps in keeping Vbias constant even if there are changes in the power supply.

Insimplewords,thisbiasingcircuitactslikea backbone of the system. It ensures that the voltage remains fixed, the current is controlled, and all parts of the circuit work smoothly without any disturbance. Becauseofthis,theoverallsystembecomesmorestable, reliable, and accurate. So, this DC response not only explainshow the circuitbehaves butalso proves that the design is working correctly and efficiently as expected.

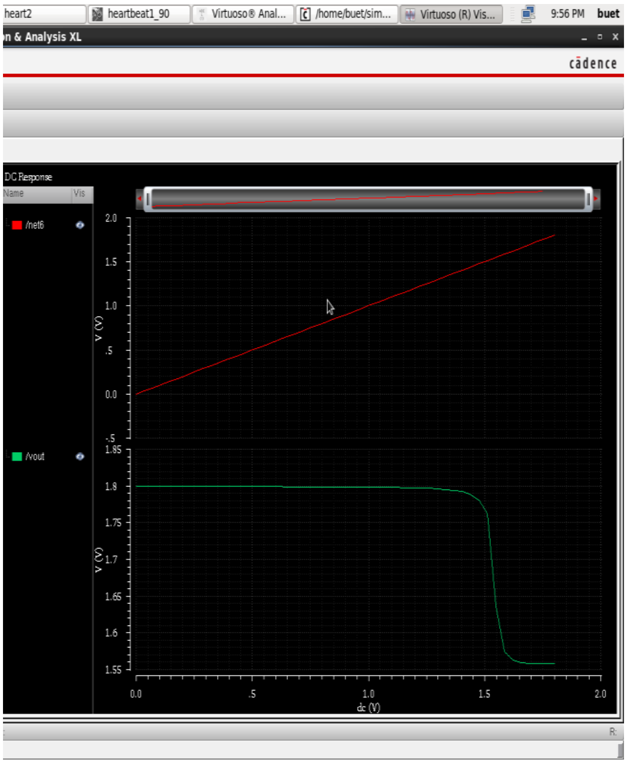


Figure6:DCResponsesofBiasingCircuit

9. TestSchematic&DCresponseofComparator circuit

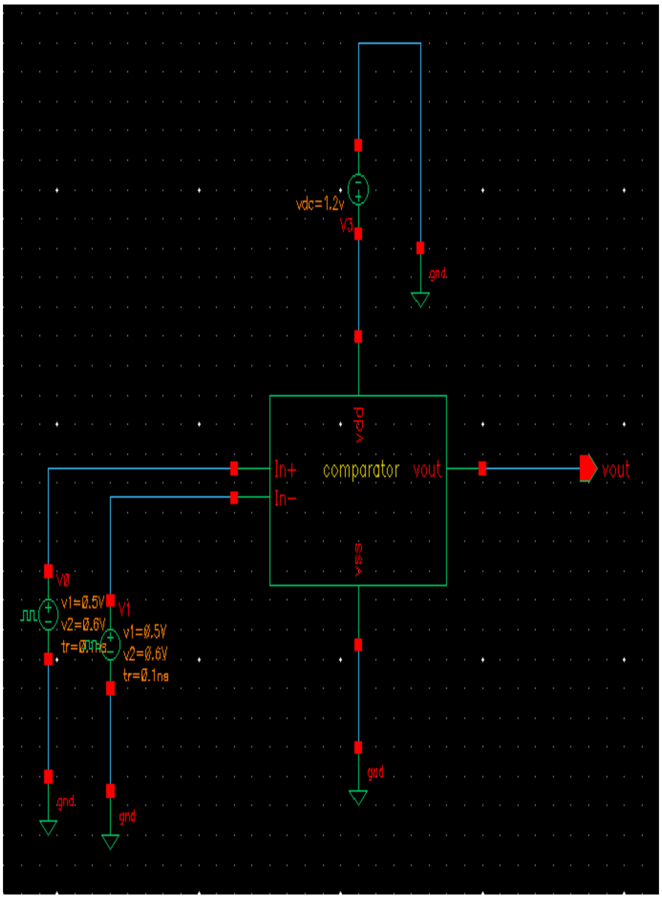


Figure7:Test schematicofComparatorCircuit

Inthisdesign,thecomparatorplaysaveryimportantrole by continuously comparing two input signals, namely IN+ and IN−, and giving a clear output based on which signal is stronger. Its operation is simple but very powerful. It works like a decision-making block that checks both inputs at every moment and produces a binaryoutput, either high or low. If thevoltage atIN+ is greater than IN−, the output goes high, and if IN− is greater than IN+,theoutputgoeslow. Thiskindofhigh- or-lowactionhelpsinclearlyidentifyingevenverysmall differences between the two signals. Even a slight variation in input is enough to change the output, which shows how sensitive and responsive the comparator is.

This sensitivity is especially useful in applications like PLL readout systems, where accurate timingandphasecomparisonareveryimportant.Insuch systems, the comparator helps to identify which signal arrives earlier or which one is stronger. This is directly related to measuring timing differences and understanding the delay introduced by components like thedelaycell.Becauseofthis,thecomparatorbecomesa key block in analyzing phase differences and ensuring proper synchronization in the system.

Anotherimportantfeatureofthecomparatoris that it converts analog inputs into a digital output. The input signals IN+ and IN− can be continuous analog signals, but the output is always in a clean digital form, either high or low. This makes it very easy to connect withthenextstagesofthecircuit,whichusually workin digital logic. So, the comparator acts like a bridge between analog and digital parts of the system.

In addition to this, the comparator helps the system to clearly distinguish between signals and make correctdecisionsbasedontheirvalues.Itensuresthatthe comparisonprocessisaccurateandreliable.Thisdirectly affects the performance of the PLL readout system, because correct comparison leads to proper phase detectionandstableoperation.Ifthecomparatordoesnot work properly, the entire system may give incorrect results or become unstable.

In simple words, the comparator is a very essentialblockthatcheckswhichsignalishigher,detects small differences between inputs, and gives a clear high orlowoutput.IthelpsthePLLsystemunderstandtiming differences,performaccuratecomparisons,andmaintain stableandreliableperformancethroughouttheoperation. It also improves the overall speed of the system because it quickly responds to even tiny input changes without delay. This fast switching behavior helps in real-time signalprocessing,whichisveryimportantinapplications likebiomedicalmonitoring.Thecomparatorensuresthat small signal variations are not missed, which increases the accuracy of the system.

In this design, the DC response of the comparator clearly explains how the circuit behaves when the input voltage changes, and it gives a clear understanding of its working in a practical way. At the initial stage, when the input voltage is very low, the output of the comparator remains in a HIGH state, which is approximately around 1.2V.Thishappensbecausetheinputvoltageisstillbelow the internalreferencevoltageof thecomparator. Since the comparator continuously compares the input with this reference, it keeps the output HIGH as long as the input does not cross that level. This region shows that the comparator is stable and does not react unnecessarily to very small or insignificant input variations. This is very importantinrealcircuitsbecause itavoidsfalsetriggering due to noise or minor disturbances.

Astheinputvoltagegraduallyincreases,iteventually reaches a critical value known as the threshold voltage, which is around 0.7 V in thiscase. At this exact point, the comparator detects that the input has reached or slightly exceededthereferencevoltage.Themomentthishappens, theoutputdoesnotchangeslowly;instead,itswitchesvery quicklyfromHIGHtoLOW.Thissharptransitionisakey characteristic of a good comparator. It shows that the circuit is highly sensitive and can respond immediately to small differences between the input and reference signals. The switching is almost instantaneous, which makes the comparator very useful in high-speed and timing-based applications.

The steep drop observed in the output waveform is verysignificant.Itconfirmsthatthecomparatorisworking correctly and efficiently. A proper comparator should always show a clean and sudden transition rather than a gradualchange.Iftheoutputchangedslowly,itcouldlead touncertaintyindecision-makinganderrorsinthesystem. Buthere,theabsenceofoscillations,noise,orintermediate levels indicates that the comparator has strong gain and gooddesignquality.Thiskindofbehaviorensuresthatthe output is always clearly defined as either HIGH or LOW, without any confusion.

This behavior also proves that the comparator has good noise immunity. Even if there are small fluctuations around the threshold, the comparator does not produce unstableoutputs.Instead,itmakesacleardecisiononcethe input crossesthe reference level. This isvery importantin applications like PLL readout systems, where accurate timingandphasecomparisonarerequired.Asmallmistake in detection can lead to incorrect system behavior, so this sharp switching helps maintain accuracy.

In simple words, the comparator acts like a fast decision-making switch. It keeps the output HIGH when the input is below the reference and immediately changes ittoLOWwhentheinputcrossesthatreference.Thisquick and clean transition helps in detecting threshold levelsthe understanding signal timing differences, and ensuring reliable operation of the overall system. Because of this strong and stable performance, the comparator becomes a very essential block in circuits that require precision, speed, and accurate signal comparison.

In addition to this, the comparator’s behavior also shows how efficiently it can be used in real-time signalprocessingapplications.Sinceitreactsinstantlyat the threshold point, it helps in detecting exact switching moments without delay, which is very important for synchronization in PLL systems. This precise switching ensures that timing errors are minimized and the system can accurately track phase differences between signals. Moreover, because the output is always a clear HIGH or LOW, it simplifies further processing stages and avoids confusionindigitallogic.Overall,thiskindofclean,fast, and reliableresponse makesthecomparator astrong and dependable component in maintaining the accuracy and stability of the entire circuit. This characteristic also showsthat the comparator canhandle variations in input signals without losing its accuracy. Even when the input changes slowly or is affected by small disturbances, the comparator waits until the exact threshold is reached before switching, which ensures correct decision-making.Thispreventsunwantedswitchingandimproves theoverallreliabilityofthesystem.Becauseofthisstable and controlled behavior, the comparator supports consistentperformanceindifferentoperatingconditions, making it very suitable for sensitive applications where precision and stability are very important.

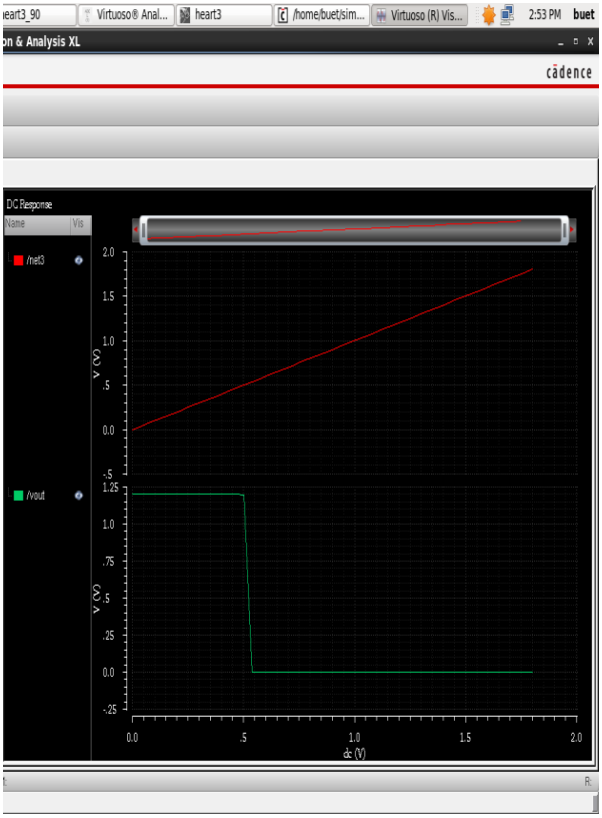


Figure8:DCResponsesoftheComparator

10. Result

This is the test schematic of the delay cell designed in Cadence Virtuoso. The input pulses applied through the VPULSEsourcestestthebehaviorofthedifferentialdelay cell. The DC voltage sources VDC bias the circuit by providing constant biasing voltages such as VP, VC, and Vbias, ensuring that the transistors inside the circuit are working properly. The differential outputs are taken from thedelaycell,Vout+andVout-,toobservethetime delay between the input and output waveforms. Such a setup helps in the analysis of the delay and waveform shape, thereby characterizing the performance of the delay cell under given biasing conditions.

InputSources

Twoinputpulsesareapplied:

→0Vto1.2 v

→SameasIn$^+$butcomplementary(oppositephase)
Thisdifferentialinputhelpsinnoisecancellationandgives a balanced output

PulseParameters

Period:40ns→correspondsto25MHzfrequency(since)

Pulse width: 20 ns →givesa 50 % duty

1nsandFalltime:1ns
These values are chosen so that the signal changes at a moderateratefastenoughtotestdelaybutslowenoughfor clear waveform observation.

WorkingPrinciple

When and are applied, the delay cell produces differential outputsand the Vbias, Vp,andVcprovidethecorrectDC operating point so that transistors stay in active region.

ResultInterpretation

The waveform output at 45 nm is curved- edged since faster charging and discharging of the transistor switches. Thewaveformoutputat90nmismoresquarebecausethe transistorswitchingisslower.Hence,delayat45nmis≈ 17.3ns,whichissmallercomparedwiththedelayat90 nm,whichis≈51ns.

In90nmtechnology,thelengthofthetransistor channelislarger,about100nm.Thelargerthechannel,the less the current that is flowing through the transistor, and thegreaterwillbetheinternalresistance-capacitance product.BecauseofthishigherRCdelay,thechargingand dischargingoftheoutputnodehappensslowlyandsteadily. When a signal switches, it takes longer toreach the final logiclevel(0Vor1.2V).Thisisbecausethisslower transition allows the waveform to fully settleat eachlevel beforeswitchingagain.Asaresult,theoutputsignal maintainsaflattopandbottom,appearingsquareor rectangular in shape.

In this process, both the PMOS and NMOS transistors have enough time to drive the output fully, producing sharp transitions. Because of the longer channel, the switching speed is lower, and therefore the propagation delay (the time between input and output change) is larger about 51 ns in our observation. Thus, the waveform in 90 nm is perfectly square since the transitionsof signalare slower butstable, whichpermits complete charging and discharging in each cycle.

Inthe45nmtechnologynode,thechannellengthof the transistor is smaller, at about 45 nm. The shorter channel will increase the drive current of the transistor and decrease the RC delay. Due to this high speed, the charginganddischargingofthenodecapacitorhappenso quicklythatthesignaldoesn’tgetenoughtimetoremain flat at each level.

This quick movement gives curved edges at the risingandfallingportionsinthewaveform,whichappear rounded or exponential instead of straight. Here, the PMOSpull-updeviceisslightlyweaker;hence,therising edge appears more curved due to charging, whereas the NMOS pull-down device is stronger and gives a sharper falling edge. That is why this waveform looks partly curved and partly square. Because of this faster switching,thepropagationdelayismuchsmalleraround 17.3nsandpowerconsumptionisalsoreduced.

The45nmwaveformiscurvedsincethetransistors switch so fast that the node voltage cannot stay flat. In contrast, the 90 nm waveform is square since slower transitions permit complete charging and discharging.

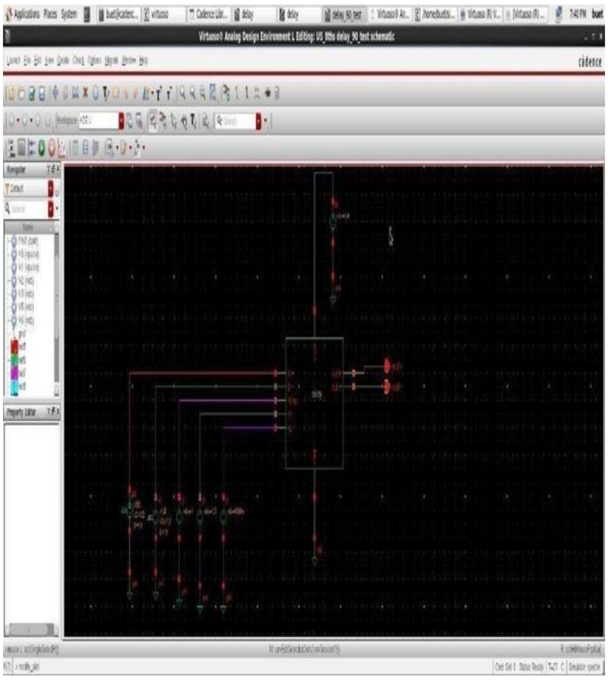


Figure9:TestSchematicofdelaycell

Waveforms

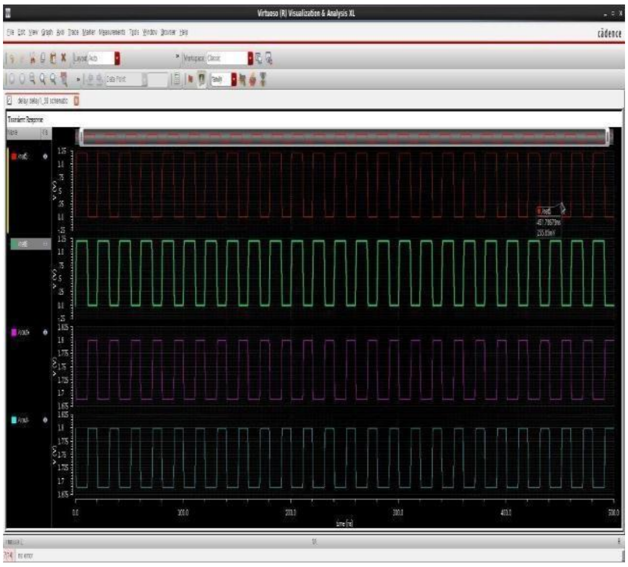


Figure10:Delaycell(90nm)

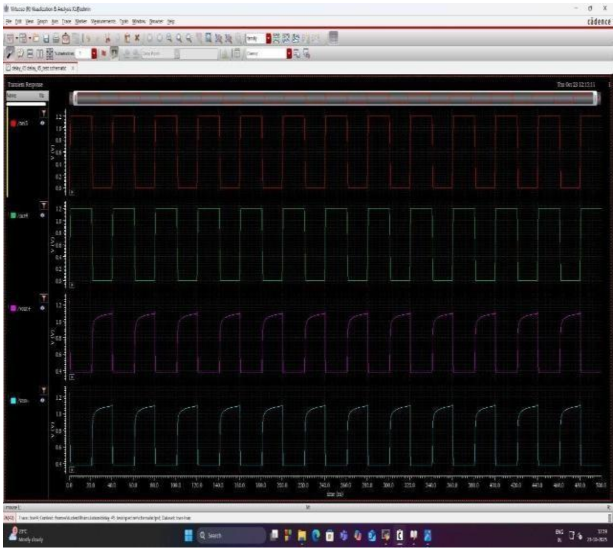


Figure11:Delaycell(45nm)

The DC bias voltages used in the delay cell design are carefully selected for both 45 nm and 90 nm technologies inordertomaintainpropertransistoroperationandachieve accuratedelaymeasurement.Inthe45nmtechnology,the bias voltages are set as Vbias = 1.8 V, which is used to establish the required bias current for the NMOS transistors, ensuring that they operate in the saturation region for stable performance. The control voltage Vc is alsosetto1.8V,whichplaysakeyroleintuningthedelay by controlling the effective switching behavior of the transistors. Similarly, Vp = 1.8 V is applied to the PMOS load network to maintain proper load conditions and balance the circuit operation. The supply voltage Vdd is chosen as 1.3 V, which is comparatively lower due to technology scaling, helping in reducing power consumption while maintaining performance. A threshold voltageof0.65Visusedasareferencepointformeasuring delay, which represents the midpoint of signal transition.

For the 90 nm technology, the bias voltages are slightly different due to larger device size and different operating characteristics. Here, Vbias is set to 1 V to control the NMOS bias current, Vc is maintained at 1.2 V for delay tuning, and Vp is set to 0.9 V to bias the PMOS loadnetwork.ThesupplyvoltageVddisslightlyhigherat 1.4Vtosupportproperswitchinginlargertransistors,and thethresholdvoltageusedfordelaymeasurementis0.7V. These voltage values ensure that all the transistors remain in the correct operating region and provide a stable DC operatingpointforthecircuit.Theproperselectionofthese bias voltages is very important because even a small variation can affect the delay, power consumption, and overall performance. The working principle of the delay cell is based on applying differential inputs, The bias voltages Vbias, Vp, and Vc ensure stable operation by maintaining proper current flow and voltage levels across the transistors.

The working principle of the delay cell is based on differential signal operation, where two complementary input signals are applied, and corresponding differential outputs are generated. The bias voltages Vbias, Vp, and Vc together ensure that the transistors conduct properly and maintain balanced operation. When the input signal is applied, the circuit responds by producing an output signal afteracertaintimedelay,whichismainlyduetothecharging and discharging of internal capacitances. The delay is measuredbyobservingthetimedifferencebetweentheinput signal and output signal at the point where both cross a predefined threshold voltage. This method provides a consistent and reliable way to calculate propagation delay, whichisveryimportantinPLLsystemsfortimingandphase analysis.

Fromtheresultinterpretation,itisclearlyobservedthat thewaveformcharacteristicsdiffersignificantlybetween45 nm and 90 nm technologies. In the 45 nm technology, the outputwaveformshowscurvededgesbecausethetransistors switch faster and the charging/discharging process happens more smoothly due to reduced channel length and lower parasitic capacitances. This results in a faster response and improved performance. On the other hand, in the 90 nm technology, the waveform appears more square-shaped, indicating relatively slower switching and more abrupt transitions. This is mainly due to larger device size and higher capacitance, which slows down the charging and discharging process. As a result, the delay in 45 nm technologyisapproximately17.3ns,whichismuchsmaller comparedtothedelayin90nmtechnology,whichisaround 51ns.Thiscomparisonclearlyshowsthatas thetechnology scales down, the speed of operation increases and delay reduces significantly. Hence, 45 nm technology provides betterperformanceintermsofspeedandefficiency,making it more suitable for high-speed VLSI and PLL applications.

Layout

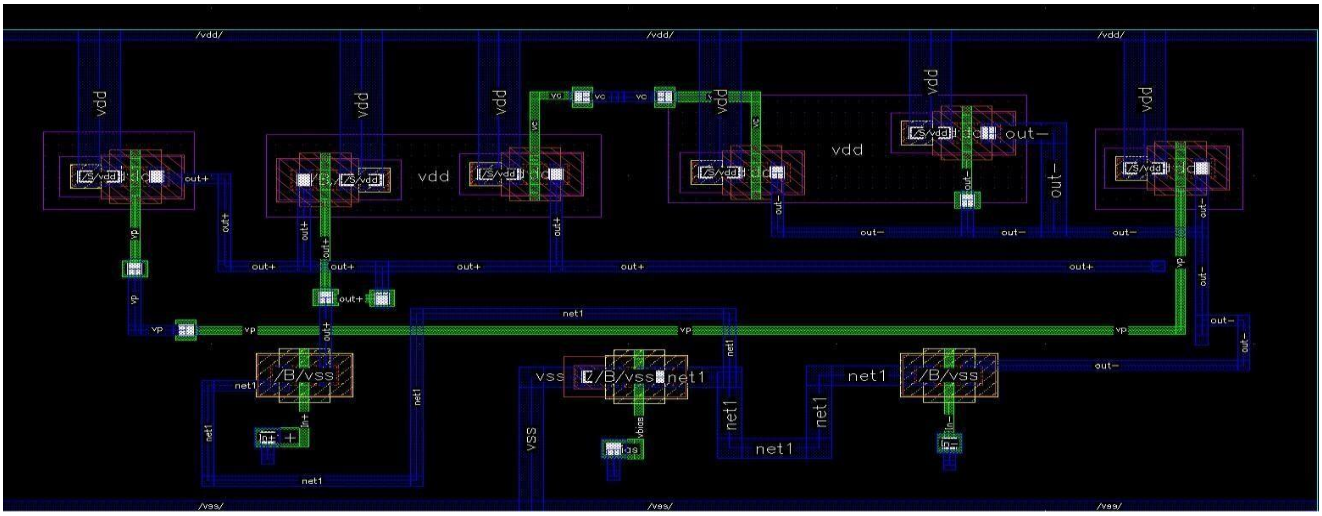
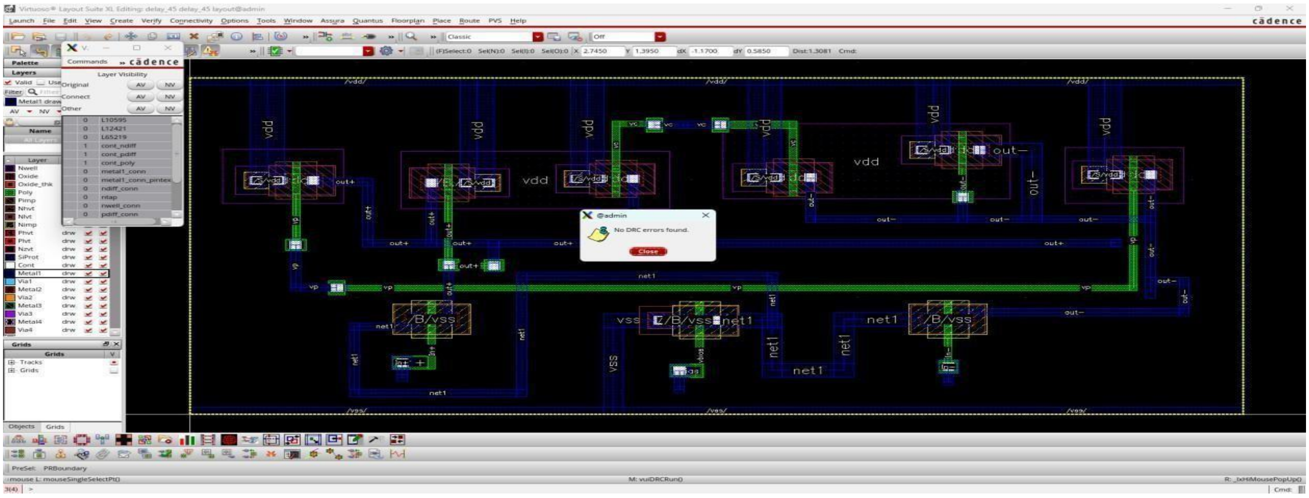
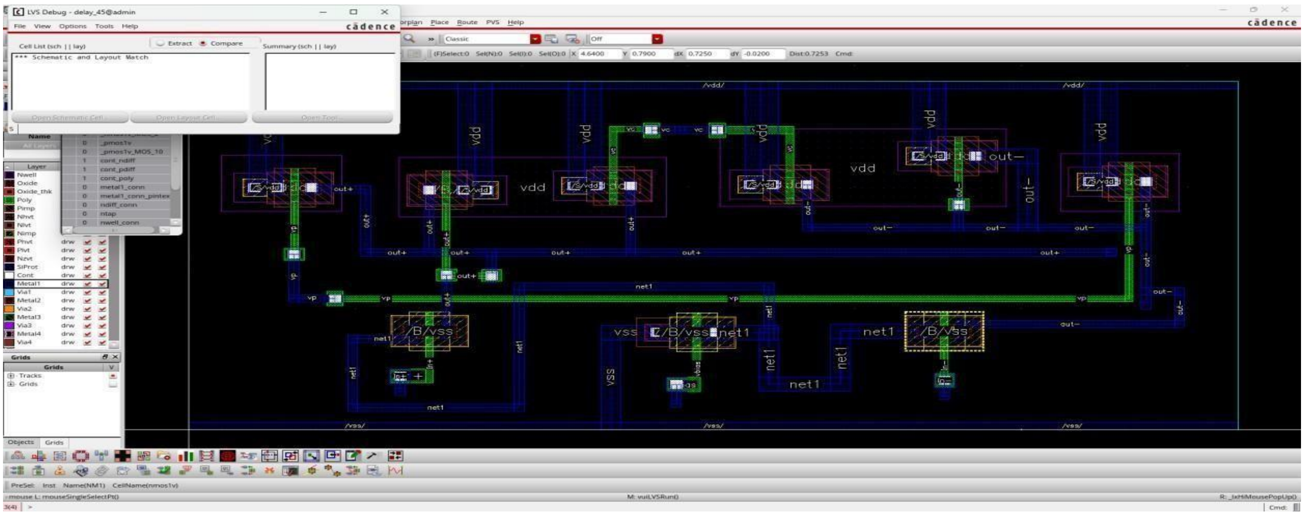


Figure12:DelayCellLayout



No DRC errors found.

Figure13:DRCtest



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*** Schematic and Layout Match
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Figure14:LVStest

In our project, the delay cell is considered as the main functional block since it is responsible for generating and controllingthedelayinaPhase-LockedLoopsystem.The biasingcircuitandcomparatorcircuitaredesignedonlyfor supporting and stabilizing the operation of the delay cell itself. They are not integrated together in our design, but rather serve to verify and analyze how each part will behave individually before integration into a complete system

The Layout design was performed only for the delay cell because it is the most critical block, which definesthetimingcharacteristicsofthesystem.Itinvolves the arrangement of PMOS and NMOS transistors, polysilicon gates, diffusion layers, and metal interconnections.

Accordingtodesignrules.Layoutwascarefully optimizedforminimumarea,symmetry,andproperrouting to minimize parasitic effects for an accurate delay performance. DRC and LVS checks were done using Cadence Virtuosoafterthecompletionofthe layout.Both checks were flawless, confirming that the layout was exactly matching with the schematic design and followed allfabricationrulesofthechosentechnologynode(45 nm).

Thus, the design, simulation, and layout verification of the delay cell conclude our project successfully.Theintegrationpartofthedelaycellwiththe biasing and comparator circuits was not implemented becauseourmaingoalwastoverify the functionality and performance of the individual circuits at the design level.

AreaMeasurement

Thetotallayoutareaiscalculatedusingtheruleror areatool inCadenceVirtuoso.Approximately,theareaofthedelay celllayoutisaroundXμm×Yμm(mentionyourobserved valueifavailable).Keepingtheareacompactwasachieved by having short interconnections and a minimal use of metal layers, which in turn helps reduce parasitic capacitance and enhances speed. Thus, the layout is efficient,compact,andfreefromerrors,henceassuringthe successful implementation of the designed delay cell

DelayCellinPLL

Thedelaycellisoneofthemostimportantbuilding blocks in a PLL circuit. A delay cell is used to produce small, controlled time delay between signals to generate and maintain proper timing synchronization within the PLL. ThedelaycellisdesignedusingsymmetricalPMOSloads andNMOStransistors.ThebiasvoltageVbiascontrolsthe operation of these transistors. The Vbias determines the amount of current flowing through the transistors. Asthe currentchanges,thecharging and discharging time of the internal nodes also change. This directly controls the amount of delay produced by the cell.

WorkingPrinciple

The Vbias voltage controls the speed at which the transistorsconduct.WhenVbiasincreases,thetransistors allow more current to flow, which results in faster charging/discharging of the internal capacitances-thus smaller delay. When Vbias decreases, the current flow reduces, causing slower charging and discharging and hence a larger delay.

WhyDelayCellGivesSmallTimeDelayinPLLAThis way, desired timing in the PLL can be achieved by preciselytuningthedelaytimeofeachcellthroughVbias variation.Why Delaycell givessmalltime delay in PLL Adelay cell gives a small time delay since the transistors chargeanddischargethesignalveryfast.Thepropagation delayforsuchacircuitwoulddirectlydependonhowfast theinternalnodescanswitch.betweenlogiclevels0and 1. Since the transistors used are ofsmalldimensions and operateathighspeeds,the time required for this charging and discharging process is very short. Hence, each delay cell contributes a small and precise delay, and by connecting multiple delay cells in a chain, the PLL can generate the required phase shift or oscillation frequency

$$t_d = \frac{(t_{pHL} + t_{pLH})}{2}$$

td→ Represents the average propagation delay of the circuitordelaycell.Itindicateshowlongthecircuittakes to respond to a change at its input. tpHL→Propagation delaywhentheoutputchangesfrom High(1)toLow (0). It measures the falling transition delay of the output signal. tpLH→ Propagation delay when the output changes from Low(0)to High (1). It measures the rising transition delay of the output signal. Both transitions usually have different delaytimes because PMOS and NMOStransistorsswitchatdifferentspeeds. Thisgivesa balanced and accurate value for the total delay of the circuit. Purpose: It helps to evaluate the speed performance of logic gates, delay cells, or any digital circuits.

Forexample,If tpHL=
62.6
tpLH=41.0

Tofindtheoveralldelay,wetaketheaverageofboth delays: Thisgivesabalancedandaccuratevalueforthetotaldelay of the circuit. Propagation Delay: 51.0ns(45nm)

Forexample:Ift
pHL=24.15
tpLH=10.6

Tofindtheoveralldelay,wetaketheaverageof both delays:
Thisgivesabalancedandaccuratevalueforthetotal delay of the circuit. Propagation Delay: 17.0ns(90nm).

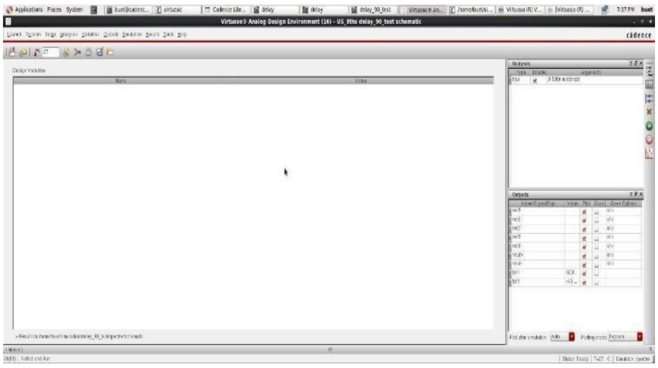


Figure15:Delayvalue(90nm)

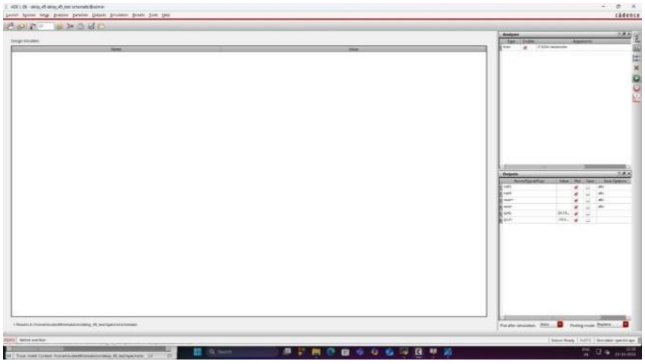


Figure16:Delayvalue(45nm)

11. ComparativeAnalysis

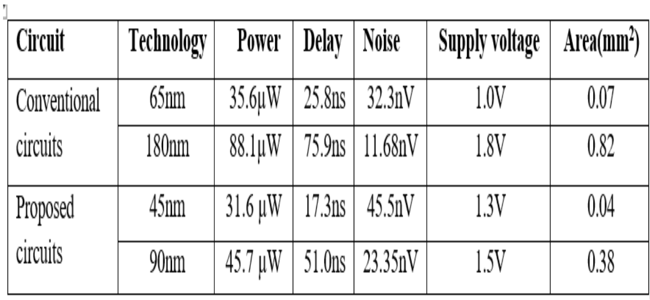
ThesearefourdifferentCMOStechnologynodes:45nm, 90 nm, 65 nm, and 180 nm. The power consumption, delay,noise,andsupplyvoltagearethekeyparametersof comparison. Each parameter illustrates how the scaling of the technology affects the behavior of the proposed circuit.

Delay

- The operating delay also shows a clear depends on upon technology size.
- The 45 nm implementation achieves the lowest the delay of 17.3 ns, because smaller transistors switch faster.
- 65nmexhibitsmoderatedelayof25.8ns.
- In90nm,thedelayincreasessignificantly51.0 ns.
- The 180 nm node exhibits the maximum delay (75.9 ns), as larger transistors have slower response time
- Thus,delayimproves(reduces)withtechnology scaling

NoisePerformance

- Noise levels tend to vary with device geometry and operating voltage.
- 45nmhasanoiselevelof46.5nV,higherbecausesmall devices often suffer from increased noise as channel area is reduced.



Circuit	Technology	Power	Delay	Noise	Supply voltage	Area(mm^2)
Conventional circuits	65nm	35.6µW	25.8ns	32.3nV	1.0V	0.07
	180nm	88.1µW	75.9ns	11.68nV	1.8V	0.82
Proposed circuits	45nm	31.6 µW	17.3ns	45.5nV	1.3V	0.04
	90nm	45.7 µW	51.0ns	23.35nV	1.5V	0.38

12. ADVANTAGES

Miniaturization: Small in size, the system is ideally implanted inside the human body. Compact in design, it does not make the patient feel discomfort, thus assuring minimum invasiveness for long-term use without interfering with daily activities.

Low Power Consumption: This operates on very low power,whichwouldprolongbatterylifeaswell asreduce the frequency of battery replacement. This is highly advantageous in implantable devices wherein surgical changes of batteries are quite difficult.

Real-time Monitoring: Keeps track of cardiac activity constantlyandupdatesinformation.Thus,earlydetection of abnormalities is possible by the doctors, who can immediately act to prevent complications.

High Precision Readout: Precise capture of heart signals minimizes any margin oferror. It enhances the reliability ofmedicaldatabyensuringbetterdiagnosisandtreatment planning.

13. DISADVANTAGES

ComplexDesignProcess: TheMEMSandPLLcircuits have tobe designed judiciously and skillfully. This fact increases the development time and requires expertise for proper and reliable functioning.

LimitedBatteryLife: Despitethelowpowerusage,the small battery capacity limits operating times. Replacement or recharging within the body may be difficult or require surgery.

14. Applications

Implantable Heart Monitoring Systems: These are used for continuous monitoring of heart status after transplantation; thus, any issues can be quickly identified,andtherecoveryoutcomecanbe improved

Next-gen Pacemakers: Advances accuracy and effectiveness in designing pacemakers, reducing the occurrenceoffine-tuningandadaptingeasilytopatients.

Wireless Body Sensor Networks: Provides remote health monitoring with implantable or wearablesensors that increase access to healthcare through telemedicine.

15. FUTURE WORK

1. **Integration of All Circuits:**In future, all three circuits(delay,biasandcomparator)canbecombined into one complete PLL readout system.
2. **Layout for Bias and Comparator:** The layout for only the delay cell has been completed so far. The bias circuit and comparator layout can be done afterwards.
3. **Post-Layout Verification**: It can be performed through post-layout simulation for all blocks, checking parasitic effects and accuracy.
4. **Using Smaller Technology Nodes**: The design can beimplementedusing28nmor22nmsoastoensure lower delay, power, and chip area.
5. **ChipFabrication:**ThecompletePLLsystemcanbe fabricated and tested on actual hardware.

16. Conclusion

The MEMS-based PLL readout system for implantable heart transplantation monitoring has been designed and simulated using90nmand180nmCMOStechnologies. The design has successfully achieved the key goals of miniaturization, low power consumption, real- time monitoring, and high precision readout, suitable for biomedical implants.

The comparison of performances done here shows explicit trade-offs between power, delay, noise, and voltage for 90nm versus 180nm. While 90nm is significantlymoreefficient andfaster,180nm is simpler indesignbutwithhigherpoweruseandslowerresponse. Suchacomparisonprovidesinsightintohowtechnology scaling may affect the performance of implantable medicaldevices.Theseresultsfromthisworkconstitutea solidbasisforextendingthesamedesignandanalysisto 45nm CMOS technology. This future step will allow performance evaluation at a smaller node to determine scaling provides significant benefits for long-term, reliable, and patient- friendly cardiac monitoring systems.

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