Comparative Analysis of SISO and PIPO Registers: Design, Area, and Power Metrics

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Abstract **-** In digital systems, registers are essential for temporarily storing and transferring data. Because of their unique features and specific uses, Serial-In Serial-Out (SISO) and Parallel-In Parallel-Out (PIPO) registers stand out among the other register architectures. With an emphasis on design processes, power usage, and space efficiency, this study thoroughly compares these two systems. The study examines the trade-offs between the high-speed data processing capacity of the PIPO architecture and the simplicity and space efficiency of the SISO architecture using simulation tools for evaluation and Verilog for modeling. The results provide insightful information and useful suggestions for choosing the best register type for systems with demanding power or performance needs.

Keywords: *SISO Register, PIPO Register, D flipflop, Area Utilization, Power, Timing.*

1. INTRODUCTION

Registers are integral components of digital systems, functioning as temporary storage units that enable data transfer between various circuit elements [1]. Their ability to store and manipulate data efficiently is vital for the smooth operation of numerous applications, ranging from basic communication tasks to advanced computing processes. Among the diverse register architectures, **Serial-in-Serial-out (SISO) and Parallel-in-Parallel-out (PIPO)** registers are particularly noteworthy for their distinct operational characteristics and suitability for specific use cases [2,3].

The **SISO register** operates by transferring data serially, handling both input and output one bit at a time. It's simple and sequential design makes it compact, energy-efficient, and well-suited for low-speed data transfer applications [4-6]. In contrast, the **PIPO register** supports high-speed data processing by enabling simultaneous input and output of multiple bits. While this parallel functionality ensures faster operation, it also increases hardware complexity, area requirements, and power consumption.

Optimizing power, space, and performance is becoming more and more crucial as digital systems develop [7]. SISO registers are perfect for low-power devices like IOT sensors since they are small and effective. PIPO registers, on the other hand they provide great throughput and speed, making them appropriate for uses like data transfer and computing. Selecting the ideal design for a given set of requirements needs an understanding of these trade-offs [8,9].

This research focuses on the **design, simulation, and analysis** of SISO and PIPO registers using Verilog as the hardware description language [10,11]. The study employs industry-standard tools like **Xilinx Vivado** and **Synopsys Design Compiler** to evaluate the designs based on critical metrics such as area, power consumption, and performance [12-14]. The findings aim to provide detailed insights into the advantages.

By exploring the strengths and limitations of SISO and PIPO registers, this study contributes to the field of digital design [15,16], emphasizing the importance of tailored design strategies to address specific use cases. Whether prioritizing compactness and energy efficiency or speed and throughput, this research supports the development of more effective and efficient digital systems [17,18].

2. REGISTER ARCHITECTURES

In digital design, D flip-flops (DFFs) serve as essential building blocks for constructing various register architectures, including Serial-In Serial-Out (SISO) and Parallel-In Parallel-Out (PIPO) registers. A D flip-flop shown in Fig.1 is a simple memory component that stores a single bit of data. It uses a clock signal to function, recording the input (D) value at the rising or falling edge and holding onto it until the subsequent clock cycle. Registers, counters, and other sequential circuits frequently use D flip-flops. They are essential for creating more intricate storage components and guarantee synchronous data transport. They are crucial in digital design due to their dependability and simplicity.

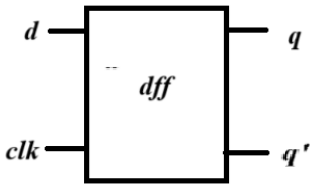

Fig.1 Basic D – Flipflop

The **SISO register** uses a series of D flip-flops connected in a linear sequence shown in Fig.2, where data is shifted one bit at a time from one flip-flop to the next. This results in lower hardware requirements but higher latency, as the data passes through each flip-flop serially before being output. The main advantages of the SISO architecture are its minimal area and power consumption, since it only requires as many flip-flops as the bit-width of the data being stored, reducing both area and dynamic power consumption. However, the serial transfer mechanism results in slower speed and limited throughput due to the number of clock cycles needed to shift data through the register.

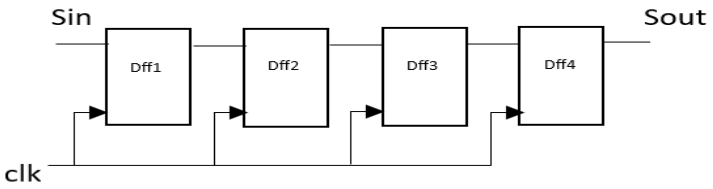

Fig.2 SISO Register using D – Flipflops

In contrast, the **PIPO register** uses D flip-flops in parallel as shown in Fig. 3, allowing data to be transferred simultaneously across all bits. Each bit of the data is stored in a separate flip-flop, and the data is loaded and output in parallel, which enables faster data transfer with lower latency. The PIPO register is particularly beneficial for high-speed applications, such as data buses, where quick data movement is essential. However, it requires more area and consumes more power, as the number of flip-flops increases with the width of the register and all flip-flops switch simultaneously, leading to higher dynamic power consumption. Both SISO and PIPO registers offer distinct advantages and limitations, with SISO being more area and power-efficient but slower. At the same time, PIPO excels in throughput and speed but at the cost of increased area and power usage. Table.1 shows the comparison between SISO and PIPO Registers.

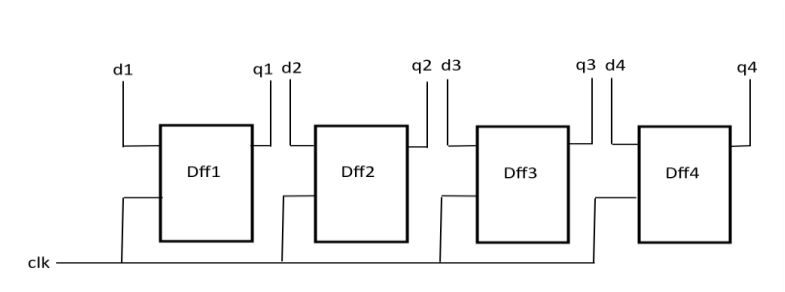

Fig. 3 PIPO Register using D – Flipflop

Table.1 Comparison between SISO and PIPO Registers

Feature	**SISO Register**	**PIPO Register**
Data Handling	Processes one bit at a time.	Processes all bits simultaneously.
Speed	Slower.	Faster.
Complexity	Simple and compact.	More complex and larger.
Power Usage	Low.	Higher.
Area Usage	Small.	Larger.
Applications	Low-speed, low-power systems.	High-speed, high-throughput tasks.

3. METHODOLOGY

This study systematically compares the SISO and PIPO register architectures, focusing on their design, power efficiency, area utilization, and performance. Initially, the registers are modelled using **Verilog**, a hardware description language that enables precise simulation of the registers' functionalities. The SISO register, designed to handle data serially, utilizes a single input and output, while the PIPO register processes data in parallel, requiring more complex control logic for simultaneous input and output. Xilinx Vivado and Synopsys Design Compiler is used for synthesis to assess the performance of both designs, enabling the generation of detailed power and area reports. These tools facilitate the accurate synthesis of the register designs, followed by evaluating area and power consumption. Key metrics such as gate count, silicon area, and dynamic and static power consumption are gathered and analyzed.

Power efficiency is evaluated through dynamic power analysis, which measures the power consumed during active data shifting, and static power analysis, which estimates power leakage when the registers are idle. These analyses are essential for understanding the overall energy efficiency of each register design, especially in power-sensitive applications. For area analysis, the area consumed by each register is calculated, using either gate count or silicon area, derived from the synthesized designs. This provides insight into how resource-efficient each register is.

Lastly, the performance of the registers is evaluated in terms of throughput and latency, using simulations and synthesis to determine how efficiently each design handles data transfer at various speeds. The methodology includes a detailed analysis of the trade-offs in power consumption, area, and performance, ultimately allowing for a fair comparison between the two register types. By implementing this methodology, the study aims to provide a thorough comparison of SISO and PIPO registers, offering key insights into their strengths and weaknesses, and helping to guide decisions based on design goals related to power, area, and performance.

4. DESIGN AND IMPLEMENTATION

In this work, **SISO (Serial-In Serial-Out)** and **PIPO (Parallel-In Parallel-Out)** registers are designed using Verilog to analyze their performance in terms of power and area. The designs were synthesized and tested using **Xilinx Vivado** and **Synopsys Design Compiler** to generate detailed reports.

SISO Register Design:

For the SISO register, a chain of **D flip-flops** are used to transfer the data serially. The data enters one bit at a time and is shifted through the flip-flops on each clock cycle until it reaches the output. This design is straightforward and efficient, consuming less power and area. The Verilog design models of this as a shift register, with sequential data movement synchronized to the clock signal.

PIPO Register Design:

The PIPO register was designed to handle parallel data transfer. Each bit is stored in a separate **D flip-flop**, enabling all bits to be loaded and output simultaneously within a single clock cycle. While this design offers higher speed, it requires more hardware resources and consumes more power. The Verilog code was written to enable parallel data operations for both input and output.

Implementation and Tools:

Both designs were described in Verilog and synthesized using **Xilinx Vivado** and **Synopsys Design Compiler**. These tools generated gate-level netlists and provided power and area reports. The SISO register showed better power and area efficiency, while the PIPO register demonstrated superior speed due to its parallel processing capability. This implementation highlights the trade-offs between simplicity and performance, with the SISO register being suitable for low-power applications and the PIPO register catering to high-speed requirements.

5. RESULTS AND DISCUSSION

SISO: For each clock pulse occurs the data at the input of the Flip-flop shifted to the output of the Flip-flop. When the clear signal is high the data from the Sin transfers to each Flip-Flop. The simulation waveform is shown in Fig. 4 and the corresponding mapped schematic from the Synopsys DC Compiler tool can be observed in Fig. 5.

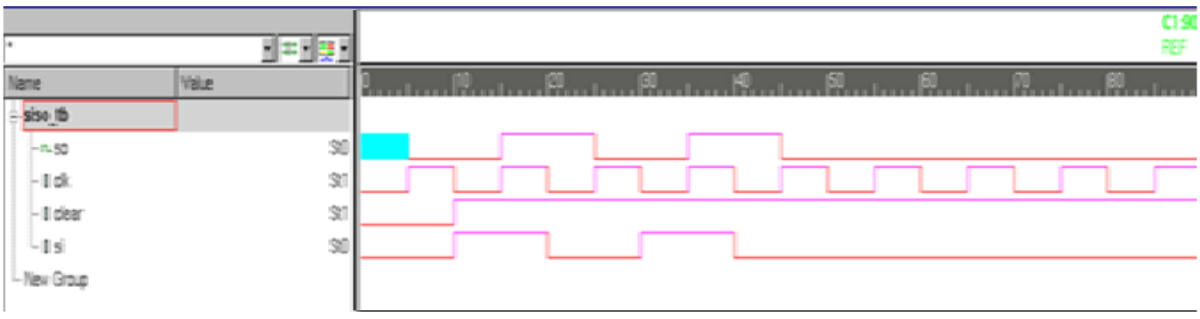

Fig. 4 Output waveform of 4-bit SISO register

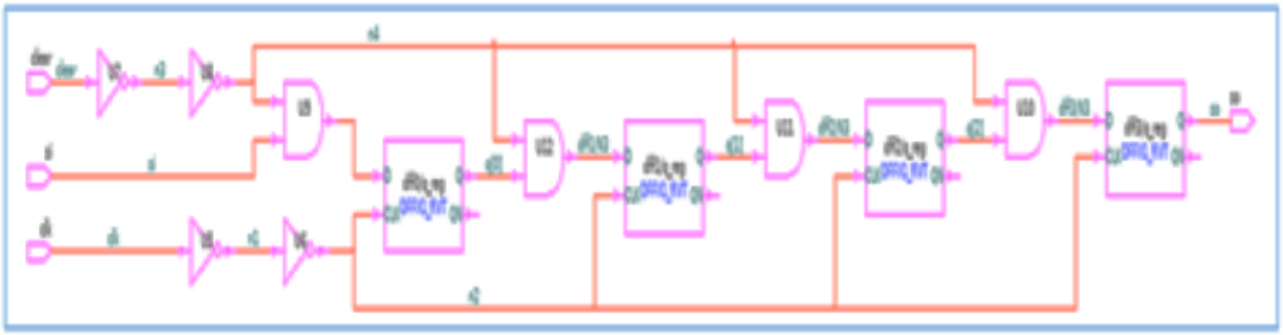

Fig. 5 Mapped schematic of 4-bit SISO register

PIPO: When the Clear signal is high and the for each clock pulse, the data at input of each Flip-Flop is transfers to the output of each Flip-Flop. The Simulation waveform for a 4-bit PIPO shown in Fig. 6 and the mapped schematic from Synopsys DC Compiler tool can be observed in Fig. 7.

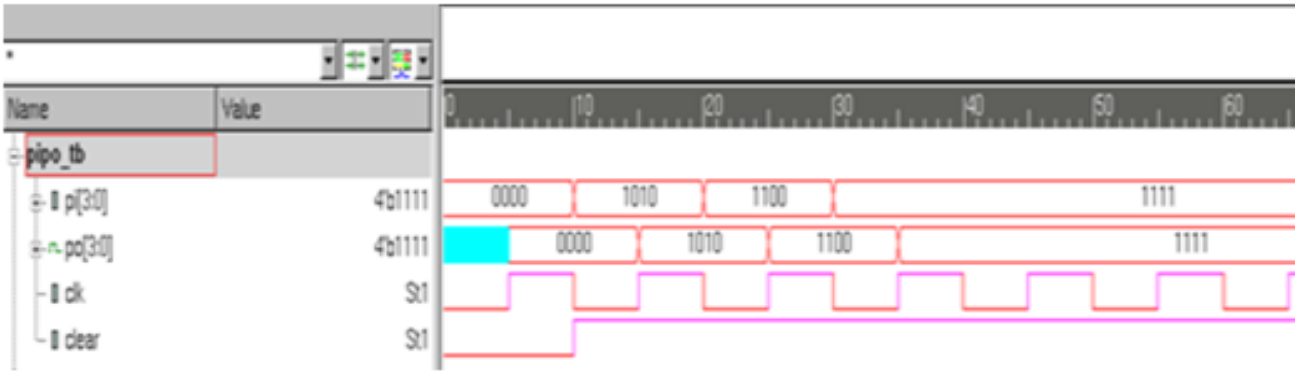

Fig.6 Output waveform of 4-bit PIPO register

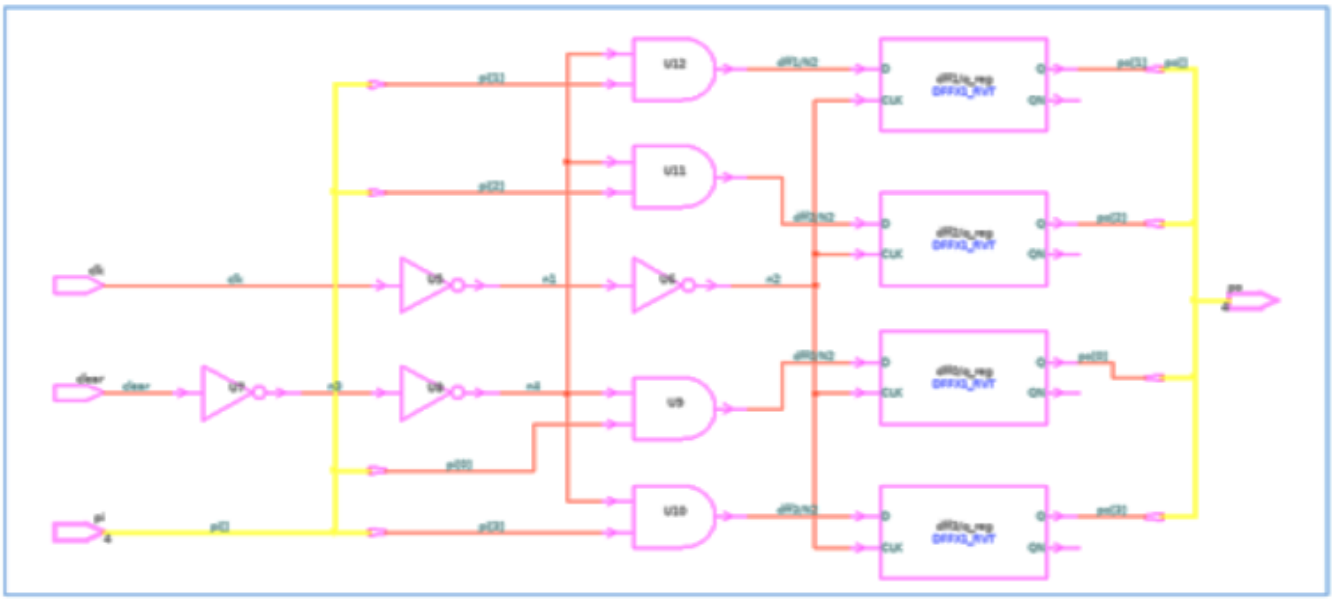

Fig. 7 Mapped schematic of 4-bit PIPO register

Comparison of SISO and PIPO:

Dynamic power and cell leakage power comparison of SISO and PIPO registers are shown in Table. 2 and Fig. 8.

POWER:

Table.2 Dynamic and Cell leakage power comparison of SISO and PIPO

	SISO	PIPO
dynamic power(µw)	1.405	1.775
cell leakage power(µw)	0.089	0.095

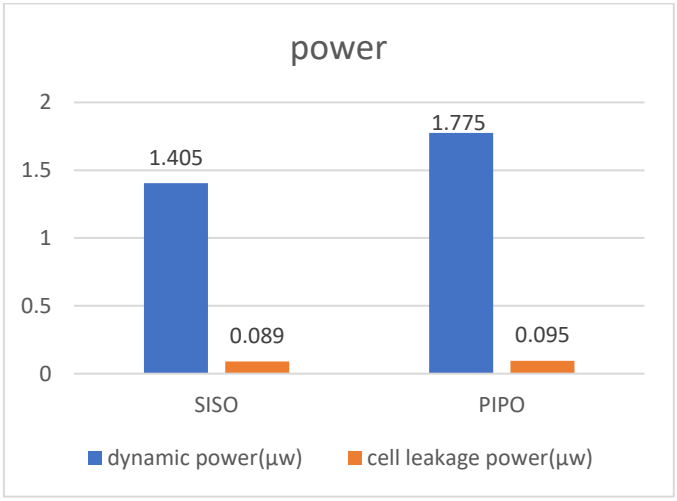

Fig. 8 Graphical Representation of Power Comparison of SISO and PIPO

Total Area and combinational area comparison of SISO and PIPO registers are shown in Table. 3 and Fig. 9.

AREA:

Table. 3 Total Area and combinational area comparison of SISO and PIPO

	SISO	PIPO
Total area (µm^2)	41.540	42.274
combinational area (µm^2)	13.215	13.945

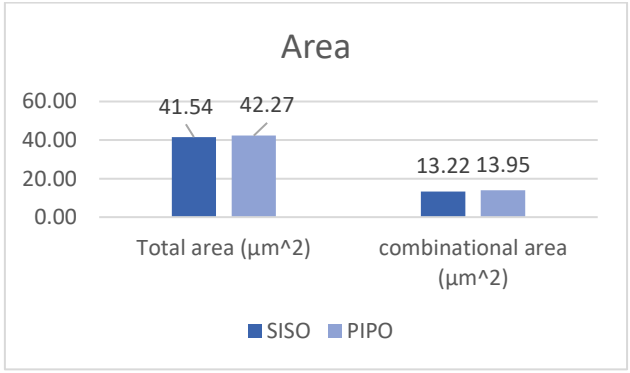

Fig. 9 Graphical Representation of Area Comparison of SISO and PIPO

TIMING:

Data arrival time of and graphical representation of SISO and PIPO registers are shown in Table. 4 and Fig. 10.

Table. 4 Data arrival time of SISO and PIPO

	SISO	PIPO
Data arrival time (ns)	0.24	0.21

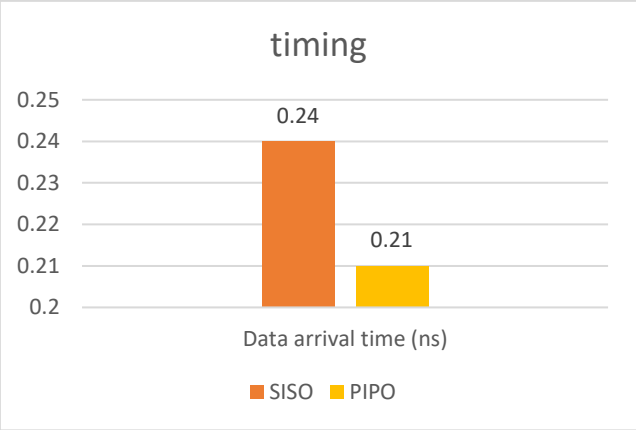

Fig. 10 Graphical Representation of Timing Comparison of SISO and PIPO

6. CONCLUSION

This study compared the design, power efficiency, and area usage of **SISO (Serial-In Serial-Out)** and **PIPO (Parallel-In Parallel-Out)** registers. SISO registers, known for their simplicity and compactness, are more efficient in power and area, making them suitable for low-power systems like IoT devices. In contrast, PIPO registers excel in high-speed operations due to their parallel data handling but require more area and power, making them ideal for high-throughput applications like data buses.

By using **Verilog** for modeling and tools such as **Xilinx Vivado** and **Synopsys Design Compiler** for analysis, the study identified that SISO registers consume less power, although their area was slightly higher due to specific implementation factors. These results offer valuable insights for selecting register architectures tailored to system needs, with future work focusing on advanced techniques like adaptive clock gating for further efficiency.

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