Review of three level inverter topologies Based on simulation in MATLAB

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Abstract

Modern power electronic systems demand efficient and reliable inverter topologies to meet diverse application requirements. Multilevel inverter topologies are trending as an alternative for medium voltage energy control. The problems associated with inverter are power quality, harmonics and grid system. This paper presents the most important topologies like diode clamped, Cascaded-H Bridge, capacitor clamped inverters. Diode-clamped, capacitor-clamped, and cascaded inverter topologies utilize various clamping techniques, such as diodes, capacitors, and multiple converters in series, respectively, to achieve multi-level voltage output with improved waveform quality and reduced harmonic distortion in power electronic systems. This paper contains comparison table of topologies based on various parameters such as load connected, source and PWM method used. Simulation results are presented to confirm the efficiency, voltage and current Harmonics of mentioned topologies.

Introduction

Inverters serve as vital components in modern power electronics, essential across various applications such as renewable energy systems, motor drives, and uninterruptible power supplies. Operating on the principle of converting DC into AC, they enable seamless integration of diverse energy sources into electrical grids while providing efficient control over electrical equipment. Fundamentally, inverters convert DC voltage from sources like batteries or solar panels into AC voltage, achieved through semiconductor devices like transistors or thyristors. By modulating switching frequency and duty cycle, inverters produce AC output signals tailored to specific application requirements. These versatile devices find extensive use across industries. They are indispensable in converting DC power from solar panels or wind turbines into AC for grid integration or local consumption in renewable energy systems. In motor drives, inverters regulate the speed and torque of electric motors by converting DC power into variable-frequency AC.

Additionally, inverters provide backup power during mains failures in uninterruptible power supplies by converting battery DC power into AC to sustain critical loads. An inverter system includes power semiconductors, DC input sources, control circuitry, and optional output filters. While inverters offer flexibility, energy efficiency, and enable renewable energy integration, they come with complexities in design and implementation, substantial upfront costs for advanced models, and potential harmonic distortion issues in AC output waveforms, necessitating additional mitigation measures. [1]

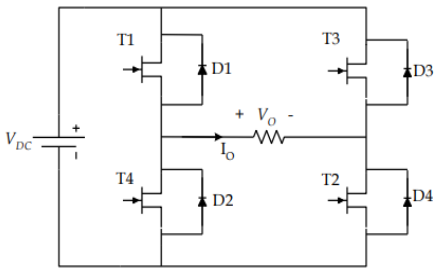

Figure 1. Basic configuration of DC to AC Inverter

In the past decade, significant progress has been achieved in multilevel inverter/converter topologies. Early and mid-1990s literature explored three traditional structures: the diode-clamped multilevel inverter developed in 1979 [2-4], the capacitor-clamped multilevel inverter or flying capacitor in 1992 [5], and the cascade multilevel inverter in 1995 [6, 7].

1. Diode clamped

Fig. 2(a) illustrates a three-level diode-clamped inverter, where the DC-bus voltage divides into three levels using two series-connected bulk

capacitors, C1 and C2, with their midpoint defining the neutral point. The output voltage, Van, exhibits three states: Vdc/2, 0, and -Vdc/2. To achieve Vdc/2, switches S1 and S2 are activated; for -Vdc/2, switches S1' and S2' are utilized, while for the 0 level, S2 and S1' are employed. Crucial components distinguishing this circuit from a conventional two-level inverter are D1 and D1', which clamp the switch voltage to half of the DC-bus voltage. When S1 and S2 are active, resulting in Vao = Vdc, D1' balances out voltage sharing between S1' and S2', with S1' blocking voltage across C1 and S2' across C2. The output voltage, Van, is AC, and Va0 is also AC. The disparity between Van and Vao is the voltage across C2, which is Vdc/2. If the output is extracted between a and 0, the circuit transforms into a DC/DC converter with three output voltage levels: Vdc, Vdc/2, and 0.

To explain the synthesis of staircase voltage, the neutral point, n, is regarded as the output phase voltage reference point. Three switch combinations are utilized to synthesize three-level voltages across a and n.

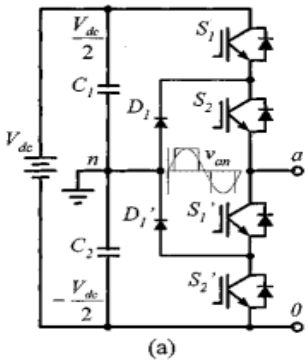

Figure 2 : (a)Diode-clamped Three level inverter circuit topologies.

2. Cascaded H-bridge

Introducing a different converter topology, this approach involves the series connection of single-phase inverters with separate DC sources [7]. Fig. 4 illustrates the power circuit for one phase leg of a nine-level inverter, comprising four cells in each phase. The phase voltage is synthesized by combining the voltages generated by the individual cells. Each single-phase full-bridge inverter produces three output voltages: +Vdc, 0, and -Vdc. Achieving this involves sequentially connecting capacitors to the AC side via the four power switches. Consequently, the resulting output AC voltage ranges from -4Vdc to +4Vdc with nine levels, and the staircase waveform approximates a sinusoidal shape even without additional filtering [1].

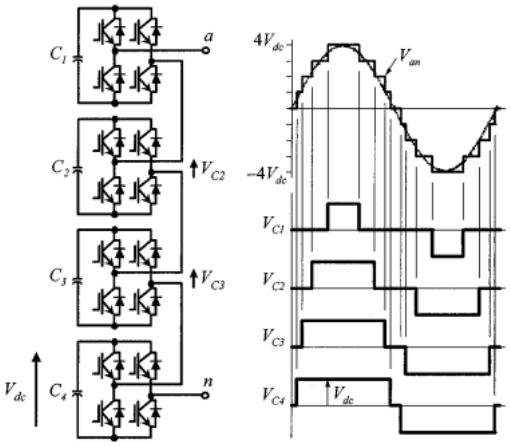

Fig. 4. Cascaded inverter circuit topology and its associated waveform.

Figure 3: Cascaded inverter circuit topology and its associated waveform.

3. Capacitor clamped

Fig. 3 illustrates the foundational component of a phase-leg capacitor-clamped inverter, commonly referred to as the flying capacitor inverter. This circuit employs independent capacitors to clamp the device voltage to a single capacitor voltage level. The depicted inverter provides a three-level output across a and n, where Van can be Vdc/2, 0, or -Vdc/2. To achieve Vdc/2, switches S1' and S2' are activated; for -Vdc/2, switches S1' and S2' are engaged, while for the 0 level, either pair (S1, S1') or (S2, S2') must be turned on. Capacitor C1 is charged when S1 and S1' are active and discharged when S2 and S2' are activated. Proper selection of the 0-level switch combination allows for the balancing of C1 charge.

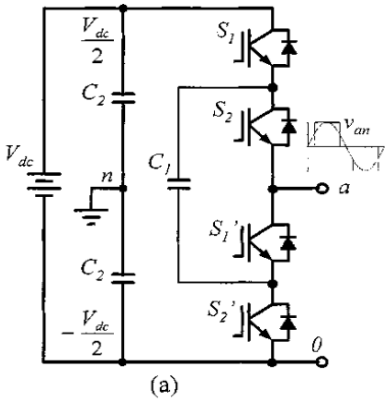

Figure 4: (a) Capacitor-clamped three level inverter circuit topologies.

PWM

1. Square

Square Wave Pulse Width Modulation (PWM) is a fundamental modulation technique extensively employed in power electronics, notably in inverter applications. It operates by toggling a power source on and off at a consistent frequency while adjusting the duty cycle to regulate the average power supplied to the load. In the context of inverters, this modulation technique is pivotal for controlling the output voltage waveform. By varying the duty cycle of the PWM signal, the magnitude and duration of the pulses sent to the inverter's switching devices are altered, allowing for precise control over the output voltage magnitude and frequency.

The operation of square wave PWM in inverters involves generating a fixed-frequency square wave signal and adjusting the duty cycle to control the inverter's output voltage. This technique finds extensive use in various applications, including motor drives, uninterruptible power supplies (UPS), and grid-tied solar inverters. In motor drives, square wave PWM regulates the speed and torque of electric motors by controlling the voltage and frequency of the inverter's output waveform. Similarly, in UPS systems, it ensures a stable output voltage during power interruptions by adjusting the duty cycle to maintain the desired voltage level. Moreover, in grid-tied solar inverters, square wave PWM facilitates the conversion of DC power from solar panels into AC power synchronized with the grid frequency. [8]

2. Sine

Sine Wave Pulse Width Modulation (PWM) is a sophisticated modulation technique commonly utilized in inverter applications to produce high-quality AC output waveforms closely resembling sine waves. Unlike square wave PWM, which generates a square wave output, sine PWM aims to approximate a sine wave output by dynamically modulating the widths of PWM pulses based on a sinusoidal reference signal. This technique involves comparing a sinusoidal reference signal with a triangular carrier wave of fixed frequency. The frequency of the reference signal dictates the output frequency of the inverter, while its amplitude controls the modulation index, influencing the amplitude of the output waveform. [8]

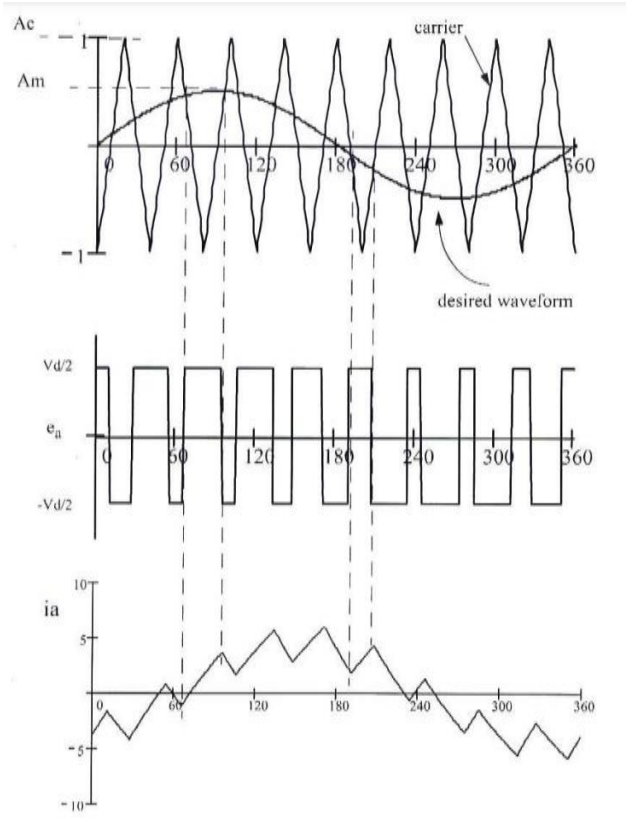

Fig.3: SPWM Technique Gate Pulses and Output Current

Simulation and Experimental Results

Simulation and experimental analysis of various multilevel topologies of 3-level inverters, incorporating both square and sine Pulse Width Modulation (PWM) techniques as switching signals, offer crucial insights into their performance across different load conditions. Beginning with detailed modelling and simulation, these studies involve the development of accurate mathematical models representing the selected multilevel inverter configurations, PWM techniques, and load characteristics, including resistive and inductive loads. Simulations facilitate comprehensive performance evaluation, covering parameters like output voltage waveform quality, Total Harmonic Distortion (THD) and efficiency.

Compare on the basis of

1. THD
2. ITHD

Topology	PWM type	Load	THD	ITHD
Cascaded	Square	R	24.58%	23.04%
Cascaded	Square	RL	23.92%	23.99%
Cascaded	Sine	R	26.2%	26.2%
Cascaded	Sine	RL	27.11%	24.71%
Diode	Square	R	26.91%	26.91%
Diode	Square	RL	27.4%	19.13%
Diode	Sine	R	26.91%	26.91%
Diode	Sine	RL	20.31%	19.06%
capacitor	Square	R	42.74%	42.74%
capacitor	Square	RL	43.90%	17.59%
capacitor	Sine	R	41.57%	41.57%
capacitor	Sine	RL	40.19%	17.00%

Table No.: 1 Comparison Table

Conclusion:

The provided data outlines the Total Harmonic Distortion (THD) and Individual Total Harmonic Distortion (ITHD) for various Pulse Width Modulation (PWM) types and loads across different topologies: Cascaded, Diode, and Capacitor. In the Cascaded Topology, both Square and Sine PWM exhibit different levels of THD and ITHD, with Square PWM generally showing lower distortion percentages compared to Sine PWM. The Diode Topology demonstrates similar trends, with Square PWM yielding lower distortion figures than Sine PWM. Notably, the Capacitor Topology consistently displays higher THD percentages across all PWM types and loads, indicating greater distortion levels. Additionally, the presence of a load (RL) influences the distortion characteristics differently across the topologies and PWM types. While RL load tends to reduce ITHD in some configurations, it often leads to increased THD, particularly evident in the Diode Topology. Engineers must carefully analyse these findings alongside other factors such as system requirements, efficiency, and cost to determine the optimal configuration for specific applications.

References:

[1] José Rodríguez, Jih-Sheng Lai, and Fang Zheng Peng “Multilevel Inverters: A Survey of Topologies, Controls, and Applications”, IEEE Transactions On Industrial Electronics, Vol. 49, No. 4, August 2002

[2] A. Nabae, et al., "A New Neutral-Point-Clamped PWM Inverter," IEEE Trans. Ind. Applicat., vol. IA-17, pp. 518-523, 1981.

[3] M. Carpita and S. Tenconi, "A Novel Multilevel Structure for Voltage Source Inverter," in Proc. EPE’91, 1991.

[4] N. S. Choi, et al., "A general circuit topology of multilevel inverter," in Power Electronics Specialists Conference, 1991. PESC '91 Record, 22nd Annual IEEE, 1991, pp. 96-103.

[5] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in Power Electronics Specialists Conference, 1992. PESC '92 Record, 23rd Annual IEEE, 1992, pp. 397-403 vol.1.

[6] F. Z. Peng, et al., "A multilevel voltage-source inverter with separate DC sources for static VAr generation," in Conf. Rec. IEEE-IAS Annu. Meeting, 1995, pp. 2541-2548 vol.3.

[7] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," IEEE Trans. Ind. Applicat., vol. 33, pp. 202-208, 1997.

[8] Anjana Thakur, Dr. A.K.Sharma, “An Overview of Different PWM Techniques to Reduce Total Harmonic Distortion of Output in H-Bridge Inverter”, Vol. 3, Issue 2, pp: (65-69), Month: April 2016 - June 2016.

[9] E. Cengelci, S. U. Sulistijo, B. O. Woom, P. Enjeti, R. Teodorescu, and F. Blaabjerge, “A new medium voltage PWM inverter topology for adjustable speed drives,” in Conf. Rec. IEEE-IAS Annu. Meeting, St. Louis, MO, Oct. 1998, pp. 1416–1423.

[10] F. Z. Peng and J. S. Lai, “Multilevel cascade voltage-source inverter with separate DC sources,” U.S. Patent 5 642 275, June 24, 1997.

[11] A. Ali Q., Awais Amin, Abdul Manan, M Khalid, “ Design and Implementation of Micocontroller Based PWM Technique For Sine Wave Inverter”, IEEE POWERENG Conference, pp 163-167, Lisbon 2009

[12] Brandon J. P., David J. P., “A Single Phase Photovoltaic Inverter Topology with a Series-connected Energy Buffer’, IEEE Transaction on Power Electronics, vol. 28, No.10, pp. 4603-4611, Oct. 2013.

[13] 5. Van Wyk, D. A. Marshall, and S. Boshoff, “Simulation and experimental study of a reactively loaded PWM converter as a fast source of reactive power, ” lEEE Trans. Ind. App1.- vol. IA-22. no. 6. pp.1082-1090. 1986.
[14] F. 2. Peng and J. S. Lai, “Multilevel Cascade Voltage Source Inverter with Separate DC Sources,” U. S. Patent #5.642.215. June 24, 1997.
[15] Z. Pan, et al., "Voltage balancing control of diode-clamped multilevel rectifier/inverter systems," IEEE Trans. Ind. Applicat., vol. 41, pp. 1698-1706, 2005
[16] L. Li, D. Czarkowski, Y. Liu, and P. Pillay, “Multilevel selective harmonic elimination PWM technique in series-connected voltage inverters,” in Conf. Rec. IEEE-IAS Annu. Meeting, Oct. 1998, pp. 1454–1461.
[17] J. Chiasson, L. Tolbert, K. McKenzie, and Z. Du, “Eliminating harmonics in a multilevel converter using resultant theory,” in Proc. Power Electron. Spec. Conf. (PESC), Jun. 23–27, 2002, pp. 503–508
[18] Ebrahim Babaei, Sara Laali, S. Alilu, “ Cascaded Multilevel Inverter with Series Connection of Novel H-Bridge Basic Unit’, IEEE Transaction on Industrial Electronics, Vol. 61, No. 12, pp. 6664-6671, December 2014
[19] M. Marchesoni, “High-performance current control techniques for applications to multilevel high-power voltage source inverters,” IEEE Trans. Power Electron., vol. 7, pp. 189–204, Jan. 1992.
[20] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, “Comparison of multilevel inverters for static var compensation,” in Con$ rec. IEEE/lAS Annual Meeting, 1994, pp. 921-928.